07/054,581 Reference 2314 A/N #4

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

APPLICANT: MICHAEL E. TOMPKINS ET AL

SERIAL NO.: CONCURRENT

FILED: CONCURRENT

FOR: SPA CONTROL SYSTEM

GROUP ART UNIT:

EXAMINER:

08/062,420 2314 2/9/94 020

PARENT 07/054,581

DECLARATION OF MICHAEL E. TOMPKINS
UNDER 37 C.F.R 1.132

Commissioner of Patents & Trademarks
Washington, D.C. 20231

Date: November 22, 1993
Docket No.: 86-1198-00

Sir:

Applicant states as follows:

1. My name is Michael E. Tompkins and I am an inventor of the above-referenced application. I am competent to give this Declaration. I am over the age of twenty-one and have never been convicted of a felony. The following statements are of my own personal knowledge.

2. I am a practicing electronic design engineer who is currently employed as the director of engineering of a medical research firm. Over the past twenty years I have been involved in every aspect of product development from the conceptual stages to final production. The fields in which these products reside include: medical ultrasound, x-ray, prosthetics, process control, industrial control, radio communications, AC and DC power management, and SCADA (Supervisory Control And Data Acquisition) systems. I am well versed in microcomputer design and am fluent in many different programming languages.

3. I have read a copy of the application that is filed in this case, copy of which is attached as Exhibit A to this Declaration. The specification is clear and exact to enable me to make and use the invention of the above-referenced application and would have enabled me to make and use the invention of the above-referenced application on May 27, 1987.

4. I was engaged by Mr. Chip Siegel who was familiar with the spa industry to manufacture and prototype the device depicted in the enclosed specification of the application of Exhibit A. I would be considered one skilled in the art of manufacturing computer control systems for applications who would work with

someone in the sales field to design computer control systems for a spa.

5. I have read the comments of Mr. David M. Ostfeld in the Appeal Brief dated February 5, 1990, in the predecessor case to this case, a copy of which is attached to this Declaration as Exhibit B. The factual statements contained in such Appeal Brief are correct. This is especially true of the knowledge of one skilled in the art described in detail on pages 9-14. These statements are correct.

6. I have also examined the examiner's answer dated July 12, 1993 to the Appeal Brief, in the predecessor or case to this case, attached to this Declaration as Exhibit C. Based on my review of the specification, attached as part of Exhibit A, the specification does adequately describe how to make and use the claimed invention. It describes the claimed invention so that the artisan could practice it without undue experimentation.

7. The entire product shown in the attached specification, attached as part of Exhibit A, was created from a preliminary design specification that was many times simpler and in no way touching any feature than the description detailed in the attached specification of the above-referenced application and in no way described any feature not in the attached specification. Also, the personnel involved in the design of the product after the preliminary design specification had no previous experience in control systems for the spa industry.

8. To say that the microcomputer was "nascent" in 1986 within the spa industry is true, which is the very reason that the descriptions of the microcomputer functions and the program were kept on a high level rather than to dwell on the characteristics and internal operations of the specific device performing the functions in the specification attached as part of Exhibit A. Any computing device ("Computers") of that period, such as microcomputer, IBM personal computer, DEC Micro-VAX mini-computer, with the proper input and output hardware as set out in the specification, attached as a part of Exhibit A, could be used to perform or execute the listed operations and algorithms contained in the

specification, attached as part of Exhibit A. An in-depth description of the computing device and its associated jargon which was old knowledge in 1987 would only detract from the details of the invention being presented in the specification, attached as part of Exhibit A.

9. The Computers had operating systems driven by real time clocks with diagnostics to trouble shoot the system, as well as drivers for operating peripherals, such as analog and digital I/O, in coordination with and scheduled by the real time clock through the operation system. Sensors were also available for many years prior to 1987 to measure pH and temperature and the state of pumps and convert such state variables into electrical signals for reading by the analog and digital I/O of the Computers. Actuators for activating heating elements were also well known years prior to 1987 and were known to be interfaceable to the digital output of computers well prior to 1987. Some of this is admitted by the Examiner on page 6 of the attached Examiner's Answer for electrical-mechanical activation.

10. I also note that computer control systems directed to solving a specific control, alarm, display problem were not the only nascent technology in the spa field disclosed by the specification, attached as part of Exhibit A, although well known in other fields. Other key devices such as triacs and optoisolators, common terms to someone skilled in the art of control, are set out in the specification but are not specifically required by the Patent & Trademark Office to be further detailed, although to my knowledge these products were used the first time in the spa industry in 1987. Until that time all previous control systems were electro-mechanical and used relays for high power pump motor and heater switching.

11. The programming language was not specified in the application of Exhibit A due to the fact that the same results could be achieved in virtually any language, e.g., BASIC, Fortran, C, Assembly, etc. Any specific language presented would possibly mislead someone not knowledgeable in the art of computer programming that this is the only language that could perform these

operations. Someone unfamiliar with that programming language if presented in the specification would have to learn that language to fully understand the specifications of the spa interaction made in the application. It is the methods of actual control of the spa that must be set out in the specification, attached as part of Exhibit A, in order to understand how to apply standard hardware and programs to solve the spa control problem.

12. As in any other fields of which I am aware that have new technology merging with existing methods, the burden of acquiring specific knowledge required to properly implement and understand this new technology, especially a field as broad as microcomputer design and programming, should be on the person knowledgeable in the existing methods. This knowledge can be provided through formal education, and user friendly software, or with the assistance of a consultant or other person skilled in the merging art. Details and descriptions not specifically related to the purpose and understanding of the control problem should be considered ancillary, unnecessary and beyond the scope of the specification teaching those knowledgeable in the existing hardware and methods how to implement the control system.

13. Real-time Clock integrated circuits that perform the task of providing the time and date to a microcomputer and to drive operating systems in some microcomputers for real time control have been commercially available since the late 1970's. The first device I used was the OKI Semiconductor MSM5832 in 1979. A similar device of this type has been used in the IBM PC since its introduction over 12 years ago. Data sheets showing the technical details of such devices are shown in Appendix D. A cursory view of these data sheets will indicate that while they all provide the time and date to a microcomputer, their internal operations are completely different. The level of detail that would be required to completely describe their internal operations and their interaction with the microcomputer would probably be longer than the application attached as Exhibit A and unnecessary to build the control system described in the specifications.

14. The term "PID" standing for "Proportional, Integral and Derivative" is a term describing a method of forming the control algorithm for and of tuning a feedback control loop in a process control system whether its electrical or mechanical. This control method and the devices performing it were exposed to me in high school electronics over twenty years ago. The term "PID" goes back to pre-1960's even before automatic electric controls when the process loop was controlled by pneumatic mechanical systems. Anyone even vaguely interested in the control of temperatures and pressures would be exposed to this term and the devices providing its function. Data sheets showing devices designed to perform PID control are shown in Appendix E. Standard control programs also existed for use with computers that implemented algorithms for "PID" long before 1987.

15. Circuitry for implementing analog to digital conversion has been around since vacuum tube days. Specific integrated circuits to provide the same function have been available since the 1970's. Once again a device was referenced as to its function and not to the specific internal operations that it performs. A pool and spa technician should understand this concept since the digital multi-meter he uses every day, and did use in 1987, provides the same function of converting an analog signal to a digital number. An in-depth description of such analog to digital converters would require details and long descriptions on items such as:

(a) type of conversion (successive approximation, dual slope integration, flash, quad slope, etc.);

(b) type of output (unipolar or bipolar);

(c) type of reference;

(d) speed of conversion;

(e) clocking (internal or external);

(f) bus interface;

(g) input impedances, etc.

These parameters are not really important to one skilled in the art in the understanding of the control system, and long subjective dissertations on why one form of converter style is better than another would detract from which analog signals are to

be converted to a digital number for control of the spa which is the information necessary for one skilled in the art.

16. Specific information on temperature sensing devices and pH probes plus input signal scanning or multiplexing and methods of providing filtering are available from many component manufacturers' data books and trade periodicals. For example, since 1964 the OMEGA Corporation of Stamford, CT publishes annually a series of handbooks, consisting of thousands of pages, which are readily available to persons in the industrial sector, to provide in-depth information on the theory, design, selection and application of sensors and their associated equipment. Appendix F contains excerpts from such handbooks showing multiplexing of analog signals for computers, noise filtering and data on temperature sensors and pH probes.

17. I hereby declare that all statements made herein of my own knowledge are true and that all statements on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so-made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity or the above-referenced application or any patent issued thereon.

Michael E. Tompkins

12-1-93
Date

DMO225:41/dgd
86-1198-06:12/01/93

CERTIFICATE OF MAILING

I hereby certify that the attached communication is being deposited in the United States mail as first class mail in an envelope addressed to Commissioner of Patents, and Trademarks, Washington, D.C. 20231, on December 1, 1993 from Houston, Texas by Donna G. Davis.

In the event that such communication is not timely filed in the United States Patent and Trademark Office, it is requested that this paper be treated as a petition and that the:

__X__ delay in prosecution be held unavoidable - 35 U.S.C. 133.

__X__ delay payment of the fee be accepted - 35 U.S.C. 151.

The petition fee required is authorized to be charged to Deposit Account No. 15-0697 in the name of David Ostfeld, P.C.

The undersigned declare further that all statements made herein are true, based upon the best available information; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

12-01-93
Date

David M. Ostfeld, Reg. No. 27,827

12-01-93
Date

Donna G. Davis
(Signature of person mailing, if other than the above)

DMO225:41/dgd
86-1198-06:12/01/93

Please place your receipt stamp hereon thereby acknowledging receipt of papers relating to the MICHAEL E. TOMPKINS ET AL SPA CONTROL SYSTEM application, S.N. CONCURRENT Filed CONCURRENT.

Respectfully,

David M. Ostfeld

Encl.-Declaration of Michael E. Tompkins Under 37 C.F.R. 1.132
Appendixes A - F
Certificate of Mailing
Return Receipt Post Card

SIEGEL/86-1198-01
DMO/dgd 12-01-93

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EXHIBIT A

1116

SPA CONTROL SYSTEM

FIELD OF THE INVENTION

This invention relates to the development of a spa control system. More particularly, this invention relates to a spa control which uses an interconnection panel and a control panel to effectively control various operating functions of the spa.

BACKGROUND

The design of systems to control spas is complicated by the environment of the spa itself. Typically, spa controls contain heating elements, controls, switches, and wiring harnesses which deteriorate when exposed to moisture or extreme levels of humidity. Since the heated water of the spa raises the humidity level, the atmosphere surrounding the controls of the spa unit is inherently corrosive to spa control systems.

The accuracy of the temperature of the spa water is essential to the safety and comfort of the spa user. This temperature is difficult to accurately control, since the temperature of the water can vary rapidly depending on the number of spa users, the ambient temperature of the air, and other environmental factors. To conserve energy, the spa temperature is customarily raised to the desired level shortly before the expected use of the spa, and is not maintained at a constant temperature. Depending on the level of use of the spa the temperature of the spa water may be cycled several times per day. During these cycles, the control of the water temperature is difficult to maintain without overheating or underheating the water. Typically, a spa control system merely heats the water with a heating element until the temperature of the water and that temperature matches a predetermined setting selected by the spa user. Since the heating element is not turned off until that desired water temperature is reached, the residual heat in the heating element may increase the temperature of the water beyond

the actual temperature desired. Conversely, the location of the temperature sensor may be located in the spa in such a fashion that it does not sense the actual, median water temperature and therefore, the heating element is turned off before the temperature of the water reaches the desired level.

Present spa controllers operate on line voltages which should not be accessible to the spa users. To meet safety specifications, these controls are typically located at a distance from the spa itself.

SUMMARY OF THE INVENTION

The present invention overcomes the foregoing difficulties by providing a spa control system which accurately and efficiently controls the operation of the spa and is not adversely affected by the corrosive environment surrounding the spa. The system monitors the temperature of the heating element and the water, and this data is processed by a microcomputer to control the temperature of the water in the spa.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 illustrates a schematic block drawing of the spa control system.

FIGURE 2 illustrates a block diagram of the microcomputer and its associated components.

FIGURE 3 illustrates a block diagram of the spa control system innerconnection panel.

FIGURE 4 illustrates a functional block diagram of the software which controls the spa control system.

FIGURE 5 illustrates one embodiment of a display.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGURE 1 illustrates a block diagram of the overall spa control system. The spa control system uses an intelligent microcomputer to monitor and control the operation of the spa. The system uses solid state electronic components which eliminate many of the problems associated with traditional mechanical timer and relay control systems. The use of solid state electronic components increase the reliability of the system and reduces the

maintained necessary to maintain the spa in operable condition.

Referring to Figure 1, the system generally comprises a spa control panel which is connected to a system innerconnection panel. The system innerconnection panel is also connected to power input, to various sensors which detect peramiters at such a slow rate, temperature, and ph of the water, and also the mechanical and electrical components of the spa, such as the pump, heater, blower, and lights.

Figure 2 illustrates a block diagram of the spa control panel and its associated components. The electronics in the spa control panel are designed to handle temperature extremes of minus twenty to plus seventy degrees centigrade. The technology used in this design is Complimentary Metal Oxide Semiconductors (CMOS) which is low in power consumption and high in reliability. The microcomputer is an 8-bit control device with an 8-bit data bus. Its function is to execute instructions, control processes, make logical decisions and compute values. The microcomputer operates at a clock speed of two megahertz and can make thousands of calculations per second. The microcomputer reads instructions from the EPROM memory and then executes the appropriate actions.

The Electrical Programmable Read Only Memory (EPROM) stores the instructions for the microcomputer to execute. Once a program is created on the development system, the final software is loaded into the EPROM. The EPROM can be modified to add new features, or additional EPROMs can be connected to manage different functions and applications. The Random Access Memory (RAM) is a memory device which stores temporary information while the information is being processed by the microcomputer. The RAM only reads and writes data, and can hold data for future reference with backup battery power even after the main power is turned off. The RAM stores data such as the number of hours on the heater, the number of times that the temperature of the spa exceeds the pre-selected temperature, and other information.

The Real Time Clock (RTC) calculates the proper time of day. The microcomputer uses this information to schedule events

concerning the operation of the spa, such as when the spa is turned on, when the water is circulated, and other events. The RTC is backed with battery power so that it maintains the accurate time when the main power supply is turned off.

The display is a vacuum-fluorescent type which has a blue-green color. The display contains four seven - segment characters, colon and a.m. and p.m. indicators. The Display Interfact represents circuitry which drives and updates the display device. Information from the microcomputer is decoded and displayed on the screen. The data remains on the screen until the microcomputer sends a new message or the system is reset or powered off.

The keyboard shown is a flat panel membrane style which is incorporated into the front panel. One type of keyboard has nine push dash buttons and nine translucent cut-offs for backlighting of Light Emitting Diodes (LEDS). The keyboard is mounted on an aluminum backpanel to provide a firm surface when depressing the buttons. The keyboard interface provides circuitry which transmits information from the keyboard to the microcomputer. The keyboard interfact conditions the signals and only permits the activation of one key at a time. The microcomputer is signaled when a key is depressed and then reads the key data.

The Digital Inputs monitors digital data from external devices, such as the flow switch. Each field digital input is optically isolated and search protected to prevent external signals from entering the main components of the microcomputer. The Digital Outputs drives the external output devices, such as the blower, heater, pump and other auxiliary devices. The low voltage signals are optically isolated and then drive a TRIAC device which provides the high voltage and high current required by the external devices. The Analog Input converts information from various sensors into digital information so that the data can be read by the microcomputer. The converter translates the analog information into digital information through dual slope integration which permits fast and accurate conversion. The

signals from external probes and sensors are conditioned by amplifying the signals so that the A-D converter can make an accurate conversion. The Signal Conditioning section provides transient and search protection to reduce static and noise.

As previously set forth, the system innerconnection panel connects the components of the spa control system. Referring to Figure 3, the power to the system innerconnection panel is supplied through usual power supply. The Ground Fault Interrupter provides protection to the system innerconnection panel if excessive current flows through the ground leg of the input. The GFI prevents excessive voltage from entering the system after the device has been triggered. After the power has passed through the GFI, the Power Supply converts the 110 or 220 Volt AC into the low voltage and low power required by the controller. The power supply also contains the backup battery used to provide power to the RTC and RAM when the main power is turned off.

The Opto-Isolators receive signals form the spa control panel which designate the operation of the proper output device. The Opto-Isolators isolate the low voltage and current control system from the high voltage and high current of the main power supply. Connected to the opto isolators are triacs, which are solid state devices used to drive high voltage and high current and high output devices. Triacs function relays except that triacs are electronic devices that do not contain any moving parts. Typically, the triac to a heating element may be rated at forty amps maximum current and the triacs to other output devices might typically be rated at twenty-five amps. Connected to the triacs is a field connection board which mechanically permits the connection and disconnection of field devices such as a pump motor, blower motor, heater core, or spa light.

FIGURE 4 illustrates a functional block diagram of the software which runs the microcomputer. The final software code is incripted on the EPROM for operating the microcomputer. The main program schedules the operation of all other subprograms and

performs general housekeeping chores, such as memory management, timer control, interrupt handling and the scheduling of tasks.

The keyboard monitor routine scans the keyboard and is triggered by the operation of a key. The key signal is then decoded and the main program is triggered to initiate a series of programmed events. The program ignores multiple key depressions and erroneous entries and operates only upon the signal generated from a proper key entry. The display control program converts data from the memory to readable messages which can be shown on the display. The display control handles the timing of the signals so that the display performs in an efficient and proper manner. The alarm control monitors the proper operation of the entire system. If the system malfunctions or otherwise operates incorrectly, the alarm will signal the malfunction. Examples of malfunctions in the system that might occur are the malfunction of the heater, and whether the PH levels are within an acceptable range. In the event of a malfunction, a signal will be sent to the display controller to alert the user of the malfunction.

The Analog Conversion Program manipulates the converter circuitry to convert sensor input signals to digital information. This program also converts the digital information to engineering units for the purposes of display and comparison. The RTC control program controls all interaction with the Real Time Clock. The program is responsible for loading data for future events. The PID Control stands for purportional, integral and derivative. This program performs the closed loop control on the heating elements. The program monitors the temperature of the water and determines when the heater should be engaged. The program issues a command which activates the heater and then monitors the temperature to determine when the heater should be turned off. The program is unique in that it monitors the rate decrease and the rate of increase of the water temperature so that the final temperature of the water is not higher or lower than the selected temperature. The spa control system can achieve an accuracy of plus or minus one degree fahrenheit with

the heating and monitoring elements.

The output control program issues commands to the output components to turn on the TRIACS for control of the pump, heater, blower, lights and other components. The input scanning program monitors devices such as push buttons and switches. The flow switch would be monitored by this program, as well as any other shut down or feed back signals. The PH ~~algarhythum~~ algorithm converts raw digital data received from the A-D converter on the PH channel and converts this data to standard PH units of measure.

FIGURE 5 shows one possible configuration of the keyboard for the spa control panel. The overlay on the spa control panel contains lights and a series of push button switches which can be depressed to switch on the appropriate functions. Preferably, an audible tone alerts the user that the computer has received the signal sent by depressing the key. The jet button operates the high speed pump for the jet action in the spa. After the jet button is depressed, the system will shut off the pump if there is no flow in the system after three seconds of operation. The user is notified of the malfunction by an error message shown on the display. In a preferred embodiment, the low speed pump automatically is operated when the heater is activated. By pressing the jet button, the high speed overrides the low pump. The heater is still operable but the heating efficiency decreases because the water is moving faster over the heating element.

The turbo button operates the blower motor for the bubbling action in the spa. The light button operates any lights installed in the spa. The up arrow button is used in conjunction with the set time, set temperature, set ready and filter buttons. The purpose of the up arrow button is to increment data that is presented on the display. The down arrow button is used in conjunction with these same buttons to decrement data that is presented on the display. The clock button is used to set the current time of day and is activated by pushing the button. The desired time can then be set by activating the up arrow button or the down arrow button. The set temperature button can be used to

control the temperature value for the thermostat in the controller. To set the temperature, the set temperature button is depressed and the current setting for the thermostat will be shown on the display. The up arrow button or the down arrow button can be used to increase or decrease the temperature setting as desired. When the desired value is shown on the display, the set temperature button is depressed and the system will revert to the normal scroll in display. The ranges on the temperature setting may range from 40 to 104 degrees fahrenheit.

The system programmer button is used to preset the time and temperature that is desired by the user. The controller calculates the proper time to initiate heating based on the present temperature of the water, and the stored data on the rate of heating for the particular spa. Each time that the spa is heated, the controller monitors the rate of change in the water temperature and stores this information in the internal memory. This data is then used to calculate the heating time.

To operate the set ready mode, the set ready button is depressed and the set ready light and the hours light digits are eliminated. The hours are set by using the up button and down button arrow. When the hours are correct, the set ready button is depressed and the minutes digits will flash. The minutes data are set by using the up button and down button arrow. When the minutes data is correct, the set ready button is depressed and the current thermostat setting is displayed. The up button or down button arrow is pressed to select the proper temperature. The set ready button is then depressed again and "on" or "off" will flash on the display screen. This indicates that the feature is enabled. The set ready button is again depressed and the system is activated. When it is time to begin the heating cycle, the system program LED flashing to indicate that the feature is active.

When the spa is heated to the proper temperature, the programmed thermostat setting becomes the current thermostat setting and the system will continue normal operation.

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If enough time is not allocated for the spa to reach the desired temperature, and time runs out before the heating process is normally completed, the programmed thermostat setting will become the current thermostat setting and the system will continue normal operation.

The filtering button allows the user to select the time for circulating the water in the spa for normal maintainance. To operate, the filter button is depressed and the hours digits and the filter light will be eliminated. The up button and down button hours are operated to select the hour, and the filter button is depressed to set the new running time. The data is loaded into memory, the filter light will turn off and the display will return to the normal scroll in operation. When the filter functions active, the LED will flash.

The heating light is eliminated when the heating element is being activated. If the heating element is activated and the temperature of the water is not increasing, then an arrow message will be displayed. The LED will flash when the heater is in the warm-up or a cool-down cycle.

The system may be diagnosed by operating a switch in the system innerconnection panel to place the keyboard in display in the diagnostics mode. By pressing the jet button, the total number of hours of operation on the pump will be displayed. Pressing the arrow button will show the total hours of operation on the blower motor. Pressing the set temp button will display the total hours of operation on the heater and will eliminate the set temp light. Pressing the time button will display the total hours the system was in an over temp state, designated as greater than 104 degrees fahrenheit in the preferred embodiment pressing any other button will eliminate the light associated with that button. Pressing the up arrow button or the down arrow button will eliminate all lights on the panel and will turn on all segments of the display along with the colon and the a.m. and p.m. indicators. The normal operation of the system is disabled when the maintenance switch is on.

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The system may display error codes which show potential problems within the system. Typical error codes which may be displayed might include information showing that the heating was not heating, the pump was not operating, there was insufficient time to heat the spa to the desired temperature, there was no water flow in the system, or there was failure in the computer.

The embodiments shown above are merely illustrative of the present invention. Many other examples of the embodiments set forth above and other modifications to the spa control system may be made without departing from the scope of this invention. It is understood that the details shown herein are to be interpreted as illustrative and not in a limiting sense.

AJA04:33

CLAIMS

WHAT IS CLAIMED IS:

1. A spa control system comprising a control panel, output components, and a heating element which heats the water in the spa, and further comprising:
   a solid state sensor for detecting the temperature of water in the spa;
   a solid state sensor for detecting the temperature of the heating element; and
   a microcomputer for processing the signals from said sensors to calculate the temperature of the water and the heating element so that the heating element controls the temperature of the water within a prescribed range.
2. A system as described in Claim 1, further comprising a Traic which drives at least one output component of the spa control system.
3. A system as described in Claim 1, further comprising an Opto-Isolator connected between the control panel and the Traics for electrically isolating the control system from the main power supply.
4. A spa control system for detecting the malfunction of components within the system, comprising:
   a display;
   a pump;
   a heating element;
   a system interconnection panel which is connected to said pump and said heater; and
   a microcomputer within said system interconnection panel for detecting the malfunction of said pump or said heating element and for generating a signal which illuminates said display to slow the

malfunction of the component.

5. A spa control system for controlling the temperature of water in the spa, comprising:

a heating element for heating the water;

a solid state sensor for detecting the temperature of the water;

a solid state sensor for detecting the temperature of said heating element;

a microcomputer for processing signals generated by said sensors to compute the temperature of the water and of said heating element, wherein said microcomputer activates and deactivates said heating element to control the temperature of said water within a selected range.

6. A spa control system as described in Claim 5, wherein said microcomputer activates said heating element to heat the water to a selected temperature without heating the water above the selected temperature.

7. A spa control system as described in Claim 5, wherein said microcomputer calculates the rate of heating of the water and said heating element, and activates and deactivates said heating element to heat the water to a selected temperature.

8. A spa control system for controlling the temperature of water in a spa, comprising:

a system interconnection panel containing a microcomputer and being connected to a power supply;

a control panel connected to said system interconnection panel;

a heating element connected to said system interconnection panel; and

a pump for circulating water over said heating element.

9. A spa control system as described in Claim 8, further comprising a heat sink adjacent said water for transferring heat from said system interconnection panel to said water.

10. A spa control system as described in Claim 8, further comprising a display in said control panel for slowing certain characters calculated by said microcomputer.

11. A spa control system as described in Claim 10, wherein said display slows a character sent by said microcomputer which identifies a malfunction of said spa control system.

12. A spa control system as described in Claim 10, wherein said display indicates the operation time of selected components of the spa control system.

AJA04:35

ABSTRACT

An improved spa control system is disclosed. The improvements may be made individually or in conjunction with any combination of all of the other improvements of the present invention. The invention describes a spa control system which calculates the rate of heating of the heater and of the water in the spa to control the operation of the heating element. The system uses a innerconnection panel to link a control panel to the power supply and to the operative components of the system. The unique connection of the control panel to the innerconnection panel permits the control panel to be located adjacent to the spa.

AJA04/34

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: "Spa Control System" copy of which

(x) is attached hereto.

( ) was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: None.

Prior Foreign Application(s)

			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	( ) Yes ( ) No
(Number)	(Country)	(Day/Month/Year Filed)	( ) Yes ( ) No
(Number)	(Country)	(Day/Month/Year Filed)	( ) Yes ( ) No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application: None.

(Application Serial No.)	(Filing Date)	(Status) (Patented, Pending, Abandoned)
		Pending and will issue to U.S. Patent 4,647,443
(Application Serial No.)	(Filing Date)	(Status) (Patented, Pending, Abandoned)

I hereby appoint the following attorney(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, with full power of substitution and revocation:

David M. Ostfeld, Registration No. 27,827
Address all correspondence to:

David M. Ostfeld
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor Michael E. Tompkins

Inventor's signature Michael E. Tompkins 5-27-87
Date

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Citizenship U.S.A.

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Full name of second joint inventor, if any Michael J. Green

Second Inventor's signature Michael J. Green 5-27-87
Date

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Full name of third joint inventor, if any

Third Inventor's signature
Date

Residence

Citizenship

Post Office Address

DMO:v42:36

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Applicant or P ntee: Michael E. Tompkins/Michae ; Green No.86-119800
Serial or Pate.. No.: Concurrent Docket No.:
Filed or Issued: Concurrent
For: Spa Control System

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.279(b) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled Spa Control System

[x] the specification filed herewith
[ ] application serial no. _____, filed _____
[ ] patent no. _____, issued _____

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

[ ] no such person, concern, or organization
[x] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME Siege Industries, Inc.
ADDRESS 1020 W. Loop North, Houston, Texas 77055
[ ] INDIVIDUAL [x] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Michael E. Tompkins	Michael J. Green	
NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
Signature of Inventor	Signature of Inventor	Signature of Inventor
5-27-87	5-27-87	
Date	Date	Date

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Applicant or Patentee: hael E. Tompkins/Michael J. Gree File No. 86-119800
Serial or Patent No.: oncurrent Docket No.:
Filed or Issued: Concurrent
For: Spa Control System

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VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[x] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN Siege Industries, Inc.
ADDRESS OF CONCERN 1020 W. Loop North, Houston, Texas 77055

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed by license to and remain with the small business concern identified above with regard to the invention, entitled Spa Control System by inventor(s) Michael E. Tompkins and Michael J. Green described in

[x] the specification filed herewith
[ ] application serial no. _____ filed _____
[ ] patent no. _____, issued _____.

If the rights held by the small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *Note: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Patricia Q. Siegel
TITLE IN ORGANIZATION Secretary/Treasurer
ADDRESS OF PERSON SIGNING 1020 W. Loop North, Houston, Texas 77055

SIGNATURE _____ DATE 5/27/87

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EXHIBIT B

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

APPLICANT: MICHAEL E. THOMPKINS §
§ ART UNIT: 243
SERIAL NO.: 054,581 §
§
FILED: MAY 27, 1987 §
§
TITLE: SPA CONTROL SYSTEM § EXAMINER: E. RAMIREZ

APPEAL BRIEF

Commissioner of Patents & Trademarks
Washington, D.C. 20231
Sir:

Date: February 5, 1990
File: 86-1198-01

On September 29, 1989, Appellant mailed his Notice of Appeal which was received by the Office on October 3, 1989. This was an appeal from the final rejection of claims 1-12, all of the claims examined in this case. Appellants further requested two, one month extensions of time. What follows is Appellant's appeal brief as required by 37 C.F.R. §1.192(a).

Status of Claims

The claims of Appellant, numbering 1 through 12 and set forth in the Appendix hereto, are pending, having been rejected by a Final Office Action dated March 29, 1989.

Status of Amendments

Subsequent to the above-referenced Final Office Action, Appellant filed a Response dated September 29, 1989, introducing testimony of the undersigned, an individual skilled in the art of real time computer control systems. The examiner responded with an Advisory Action dated October 24, 1989. In the Advisory Action, the examiner apparently entered the Response.

Summary of the Invention

The invention relates to a particular control system for controlling a spa, utilizing real time process control computers. More specifically, it relates to improvements to spa control systems to adapt their control in response to the environment of the spa. Typically, spa control systems contain heating elements, controls, switches, and wiring harnesses which deteriorate when exposed to moisture or extreme levels of humidity.

The accuracy of the temperature of the spa water is essential to the safety and comfort of the spa user. This temperature is difficult to accurately control, since the temperature of the water can vary rapidly depending on the number of spa users, the ambient temperature of the air, and other environmental factors. To conserve energy, the spa temperature is customarily raised to the desired level shortly before the expected use of the spa, and is not maintained at a constant temperature when the spa is unattended. Typically, a spa control system merely heats the water with a heating element until the temperature of the water and that temperature matches a predetermined setting selected by the spa user. Since the heating element is not turned off until that desired water temperature is reached, the residual heat in the heating element may increase the temperature of the water beyond the actual temperature desired. Conversely, the location of the temperature sensor may be located in the spa in such a fashion that it does not sense the actual, median water temperature. Accordingly, the heating element may be turned off before the temperature of the water reaches the desired level.

The present invention provides for a spa control system generally comprising a heating element, a sensor for detecting the temperature of the water, and a microcomputer for processing signals generated by said sensor and for activating and deactivating the heating element. In one embodiment of the invention, the microcomputer assesses the time necessary to heat water from an initial temperature to a selected temperature. From this information, the heating rate of the water can be calculated. The heating rate can be stored by the microcomputer and can be used to determine the start time necessary to heat the spa water from an initial temperature to a selected temperature by a desired time. In another embodiment of the invention, the temperature difference between two sensors in the spa system can be monitored to detect problems in the system. (Page 2, lines 19-31.)

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The system generally comprises a specialized spa control panel for data display and input which is connected to a system innerconnection panel for signal distribution. The system innerconnection panel is also connected to power input, to various sensors which detect parameters, such a temperature and pH of the water, and also the mechanical and electrical components of the spa, such as the pump, heater, blower, and lights. (Page 34, lines 23-28.)

The microcomputer may be of any sort and is preferably an 8-bit control device with an 8-bit data bus. Its function is to execute instructions, control processes, make logical decisions and compute values. The microcomputer reads instructions from the EPROM memory and then executes the appropriate actions. (Page 4, lines 7-14.)

The Random Access Memory (RAM) is a memory device which stores temporary information while the information is being processed by the microcomputer. The RAM only reads and writes data, and can hold data for future reference even after the main power is turned off. The RAM stores data such as the number of hours on the heater, the number of times that the temperature of the spa exceeds the pre-selected temperature, and other information.

The Real Time Clock (RTC) shows the proper time of day which is calculated after the time and date is initially set. The microcomputer uses this information to schedule events concerning the operation of the spa, such as when the spa is turned on, when the water is circulated, and other events. The RTC is backed with a battery or other well-known device (not shown) so that it maintains the accurate time when the main power supply is turned off. (Page 4, lines 18-32.)

The Digital Inputs monitor on-off, switch type data from external devices. Each field digital input is optically isolated and surge protected to prevent external high voltage, ambient electrical voltages from entering the main components of the microcomputer. The Digital Outputs drive the external spa

devices, such as the blower, heater, pump and other auxiliary devices. The low voltage signals are optically isolated and then drive a TRIAC device which provides the high voltage and high current required by the external devices.

The Analog Input converter converts information from various sensors into digital information so that the data can be read by the microcomputer. The converter translates the analog information into digital information through dual slope integration which permits fast and accurate conversion. The signals from external probes and sensors are conditioned by amplifying, filtering, or conditioning the signals so that the A-D converter can make an accurate conversion. The Signal Conditioning section provides transient and surge protection to reduce normal and common noise. (Page 5, lines 16-33.)

For the software, as with the basic, nonspecialized computer hardware, there are many standard routines known to those skilled in the art, and certain specialized programs. Generally, the keyboard monitor routine scans the keyboard and is triggered by the operation of a key. The key signal from a digital input is then decoded and the main program is triggered to initiate a series of programmed events. The program ignores multiple key depressions and erroneous entries and operates only upon the signal generated from a proper key entry. The display control program converts data from the RAM memory to readable messages which can be shown on the display. The display control handles the timing of the signals so that the display performs in an efficient and proper manner. (Page 6, line 34 through page 7, line 8.)

The Analog Conversion Program manipulates the converter circuitry to convert analog input signals from sensors to digital information. This program also converts the digital information to engineering units for the purposes of display and comparison. The RTC control program controls all interaction with the Real Time Clock. The program is responsible for loading data for

future events. The PID Control stands for proportional, integral and derivative control. This program performs the closed loop control on the heating elements. The program monitors the temperature of the water and determines when the heater should be engaged. The program issues a command which activates the heater and then monitors the temperature to determine when the heater should be turned off. Unlike the above listed programs, this program is unique in that it monitors the rate decrease and the rate of increase of the water temperature so that the final temperature of the water is not higher or lower than the selected temperature. The spa control system can achieve an accuracy of plus or minus one degree Fahrenheit with the heating and monitoring elements, (Page 7, lines 17-34) which do not require multiple temperature sensors nor any flow sensors for system operation, thereby lowering costs.

The output control program issues commands to the output components to turn on the TRIACS for control of the pump, heater, blower, lights and other components. The input scanning program monitors devices such as push buttons and switches. (Page 8, lines 1-4.)

When the system is powered up, the system is reset by system initialization, which enables certain events and calls the main program. Certain interrupts such as the timer interrupt and the power fail interrupt are enabled. The power up reset generally clears all RAM, turns off control outputs, initializes the real time clock and the keyboard scanner, tests the NOVRAM image for validity, and tests EPROM memory. (Page 9, lines 14-20.)

The controller calculates the proper time to initiate heating based on the present temperature of the water, and the stored data on the rate of heating for the particular spa. Each time that the spa is heated, the controller monitors the rate of change in the water temperature and stores this information in the internal memory. This data is then used to calculate the heating time. (Page 9, lines 21-29.)

The microcomputer processes the signals generated by the two temperature sensors located on either side of the heating element and calculates the difference in temperature between the values detected by the sensors. If the difference exceeds a selected amount, a warning on a digital display, or other warning such as an audible sound, can be generated to warn the user of a malfunction in the spa.

In addition, the microprocessor can calculate the rate of heating detected by either sensor to determine whether there may be fluid blockage in the spa system without the need of a flow sensor. This calculation can be performed by dividing the change in temperature by the change in time to compute the rate of heating. For example, if there is a fluid blockage in the system, the spa water surrounding the heating element may rapidly overheat to create a "hot spot" in the spa system. If the temperature of the water does not increase, there may be a malfunction in the heating element. If any error is detected which signifies that the spa system is not properly working, the microprocessor can deactivate the heating element to prevent overheating of the components of the spa system. The rate of heating can also be monitored to ensure that scalding water is not unexpectedly circulated in contact with the spa user.

The temperature of the water can be maintained within a selected temperature range or hysteresis when the spa is unattended. For this scheduled heating function, one start time is set, the high and low temperature limits are set, and the function is enabled. For example, the operator might select a lower temperature range in the interest of conserving energy. A lower temperature range would also reduce the number of times that the spa system would cycle on and off to maintain the desired temperature, since a lower water temperature is closer to the ambient temperature. Conversely, the operator can select a higher temperature range, closer to the desired temperature of the spa water, to minimize the time required to heat the spa water to the

operating temperature. The ability to control the temperature of the water while the spa is unattended also yields other useful benefits. (Page 12, line 4 through page 13, line 12.)

The water can be monitored to calculate the estimated time necessary to raise the water temperature to a desired level and to detect certain failure in the spa system. For example, a sudden increase in the water temperature at a specific point in the spa system may signal that there is a loss of water circulation. If a sensor detects a heating rate which exceeds a selected rate, a warning light may be illuminated, or the heating element or the entire spa system may be deactivated to prevent deleterious heating of the spa components. In addition, the rate of heating, together with the actual temperature reading and volume of water in the spa system, can be used to calculate the time required to heat the spa water to a desired temperature. This information can be stored in the microcomputer to assist in predicting the time necessary to heat the spa water to the desired temperature, beginning with the selected temperature of the water when the spa is unattended. (Page 13, line 19-35.)

Issues

Whether the Office was incorrect in determining that the present invention, which involves a spa control system which uses a standard real time microprocessor system in conjunction with specialized sensor selection and manipulators of the elements of the system based on determinations of the state of the system was unpatentable under 35 U.S.C. §112 as "vague and indefinite" because disclosure of how the microcomputer would be properly programmed to determine, for example, proper pH levels and the monitoring of temperature to determine when the heater element should be engaged, etc. was not given in the Office's opinion.

Grouping of Claims

There is only one ground of rejection, which applies to all the rejected claims.

Argument

In each Office Action, dated May 26, 1988 and March 29, 1989, the Office rejected the specification and claims 1-12 under 35 U.S.C. §112 as unpatentable. Both Actions suggest that there is an insufficient specification to permit someone skilled in the art without undue experimentation to perform the claimed invention, including converting raw signals to pH and temperature and comparing those values to preset limits to determine alarm states, as well as calculate and update rates of change and compare those to preset limits and output values. Appellant respectfully submits, however, that the specification and each of the claims at issue are such that the invention as a whole could be practiced by one skilled in the art with reasonable experimentation, mainly debugging. Claims 1-12 and the specification are believed to be allowable, and therefore the rejections of the specification and Claim 1-12 should be reversed.

The undersigned, in the final "Response", mailed September 29, 1989 to the United States Patent & Trademark Office, identified himself as one skilled in the art for this particular patent application. The undersigned has a bachelor's degree and a master's degree in control systems engineering from Washington University in St. Louis and worked for several years applying real time computer based control systems to chemical, and petrochemical and other processes, including both continuous and batch systems, all of which were more complex than a spa control system. The undersigned designed, installed and programmed and aided in the operation of these real time computer systems during the entire time while the undersigned was an engineer, including specifying sensors for these systems and the location of such sensors, wiring of those sensors into interface panels, calibrating the sensors, specifying the computer systems, both as to physical capability and programming capability, supervising the programming of such systems, and specifying the exact programs based on relatively loose functional requirements, designing

interface panels for operator usage, implementing and testing completed systems, diagnosing systems, including hardware and software, and operating processes using these real time process control computer systems. For the most part these were not microprocessor based control systems, but much larger scale computers which had features in common with the microprocessor based control systems currently available in real time applications, for which the undersigned is also familiar, having clients who use such systems and describe such systems to the undersigned during the time while the undersigned has been an attorney for such clients.

The undersigned apologizes for the length of the description in this case, but some amount of detail needed to be appreciated as to what was said in the specification to emphasize the lack of need for further description in order to determine <u>for one skilled in the art</u> if there was sufficient disclosure to implement a control system described in the specification and as set out in the claims without undue experimentation.

To the undersigned, the first thing that needs to be specified in order to purchase the microprocessor is the list of inputs and outputs, both digital and analog, and the type of memory that would be needed. All this is contained in the above specification. Indeed, not all of it need to have been contained in this specification in order to enable one skilled in the art to still have purchased the appropriate microprocessor control system knowing the type of operation in which it would be operating. All this is common to any real time computer system of the knowledge of the undersigned, and anyone skilled in the art would know how to properly configure such a system generally, including the undersigned, since at least the 1960's.

The general principles for hardware interface of the various components to the computer are also well known in the art since the 1960's based on the experience of the undersigned. For other devices that are capable if properly programmed of accomplishing

the general purposes of process control using a real time microprocessor based computer based control system, the Office should note that there are many brands available in the prior art, such as the P-100 and P-200 control systems of Powell-Process Systems, Inc. which were manufactured at least eight (8) years ago. These microprocessor based control systems have all of the features described above, except the particular control system and except for the particular interface panel and the particular control panel described in Appellant's application and the recognition of what sensors and controls were needed.

Accordingly, to run the programs would have been a matter of programming the special programs specifically described in the application into this already operating device. The fact that Appellant more generally shows a microcomputer because the preferred embodiment of Appellant is a less expensive way of commercially producing the unit than to buy an off the shelf unit already more generally programmed for which configuration of the general program to the specific control scheme would be necessary, is a commercial issue, not an issue of what is known to one skilled in the art.

Real time clocks are normally used with microcomputers in order for the computer programming ("real time monitor"), which is well known in the art, to keep track of date and time and intervals of time for turning on various programs. Real time monitors to turn on programs (whether interrupt driven through the real time clock or activated by digital scanning of the input from the real time clock) are also well known in the prior art to the knowledge of the undersigned. Accordingly, there is really no experimentation whether undue or not that is needed in order to obtain a real time computer executive system driven by a real time clock where the executive system includes a real time monitor and a scheduler to operate other programs. There is also really no undue experimentation to include a control program that includes a proportional/integral/derivative control scheme, and

an output control program, and an input scanning program, and programs for taking raw digitized analog data and converting such data to appropriate units based on well known formulas for pH and temperature inputs (depending on the kind of thermocouple or other temperature measuring device).

It is also possible without any experimentation for such a main program to scan or use an interruption from the operator's console to detect changes in state from the last input state of the console. Because the real time clock operates so much faster than a human being can react, this scanning is readily available.

No description of any of this common knowledge to those skilled in the art is needed to overburden a patent application and the expense of preparing one for anyone of ordinary skill in the art, even as early as the 1960's, much less the end of the 1980's. What is important is the sensors (temperatures), the end control device (heating element) and a brief functional description of how the calculations are made in the programs triggered by the main program.

The Office does not appear to be contesting that the part of the specification dealing with the specific unique features of the real time process control computer system of Applicant's invention do not have sufficient detail, which is the only part of the specification not old in the art and which is the part of the specification necessary to understand the progress made in the art by Applicant's invention, for those skilled in the art to implement the invention.

The Office rests its position on the words "without any description of the precise operations to be performed by microcomputer". This statement says one of three things. The first is to say that one should repeat everything that is in the prior art; i.e. to present a blue print of how to manufacture a product old in the art which is not required under the patent statute. Another position that is possible to interpret from this is that somehow the Office believes that the applicant must show the

precise code rather than describe the control system to generate that code in order to fully disclose what the programs are. Appellant submits that such a description is not required by those skilled in the art, nor is it required by the Office. Any programmer (and Appellant's undersigned attorney was such a programmer as part of his job function on occasion) can utilize a description of a program to produce a properly operating program without undue experimentation once the principles of the control scheme are disclosed to the programmer. The important thing is that the programs operate in a real time environment, manipulating real equipment to cause real time process control, which can be adequately described from a functional, not programming, description of the programs without undue experimentation.

It is not important to know what code to use if in fact the one skilled in the art has a different computer system. In fact, if one were to disclose actual codes or detailed flow diagrams for one computer system instead of the functional specifications of the programs, this would lead away from the invention because if one of ordinary skill in the art were not using that computer, then one skilled in the art would first have to learn the old code or structure, interrupt it, and then the new code would be prepared rather than just using the functional specifications of the programs to prepare the new code.

It may also be possible that the Office is saying that techniques were not known in the prior art for converting the readings of a pH level device or a thermocouple or other temperature device or to calculate a rate of change or to recalculate batch reaction or heating times and when to perform these. This is not true of the undersigned's own knowledge and experience.

The key is to know which temperature changes and which temperatures are to be used for such calculations and generally how such a calculation is to take place to enable one skilled in the art to make such a calculation.

Further, it may also be possible from the words used by the Office, "or to coordinate the other system components and the proper time sequence to perform the functions disclosed and claimed" that the Office is saying that those skilled in the art would not know how to configure a real time process computer system to repetitively scan the temperature to then make the determination set out in the program. This is also not correct.

Scanning by times or by fixed or variable intervals of variables by a real time clock driven microcomputer control system are well known in the prior art based on the undersigned's own knowledge. See the P-100 and P-200 computers. As the undersigned has stated as one skilled in the art, those are readily known factors that anyone skilled in the art of real time process control would not doubt as to how to perform without undue experimentation in order to scan the temperatures in order to make the test and reaction fully described in the application.

As set out above, the key is the elements to be used in the control system. As set out in claim 1, and in the specification, the two sensors on either side of the heating element are unique, permitting the prediction of freezing, as well as prediction of changes in characteristics of the spa through determination of time per degree temperature rise for heating using the heating element which can be used adaptively by substituting in those times in the next calculation for when to turn on the heating element in order to bring the spa to a given temperature at a given time from a measured starting temperature. It is also a fairly easy calculation to determine the difference between the temperature of two places across the heating element to calculate if that difference is excessive or to monitor one temperature to detect failures to rise quickly, thereby indicating a heating element that is not operating properly. The key is that by doing this, one ordinarily skilled in the art would recognize there is no need for a flow indicator. Further, to calculate change in temperature of a single heating element over a period of time is

not difficult and is described in the specification as a differencing of that temperature at two different times, and is adjustable as to a time interval without undue experimentation with the actual spas involved and dividing it by the time interval. Most of the alarms are set on an adjustable basis from a particular spas involved. The need for flexibility and inputting this data is recognized in the specification.

A "patent application need not include in the specification that which is already known to and available to the public". Paperless Accounting, Inc. v. Bay Area Rapid Transit System, 804 F.2d 659, 664 (Fed. Cir. 1986); In re Horwarth, 654 F.2d 103, 105 (CCPA 1981); In re Lange, 644 F.2d 856, 863 (CCPA 1981). One does not have to include the detailed drawings on how to make a computer system in order to assert the use of a computer system or to describe certain components to be used in that computer system. Christianson v. Colt Industries Operating Corp. 822 F.2d 1544, 1561 (Fed. Cir. 1987). To describe the design of computer system for patents dealing with parts would be an impossible undertaking to expect of an applicant. Christianson v. Colt Industries Operating Corp., supra.

The legal requirement that a disclosure be enabling is set forth in the first paragraph of 35 U.S.C. §112: "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains or with which it is most nearly connected to make and use the same...". Patents are not production documents. Christianson v. Colt Industries Operating Corp., supra at 1562. The ultimate issue is whether or not the invention claimed in the application can be practiced with dimensions, tolerances and production drawings by those skilled in the art to practice the claimed invention, Christianson v. Colt Industries Operating Corp., supra. See also Lindemann Maschinenfabrik v. American Hoist and Derrick Co., 730 F.2d 1452, 1463 (Fed. Cir.

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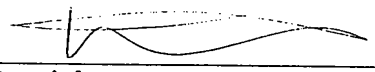
1984) and Raytheon Co. v. Roper Corp., 724 F.2d 951, 956 (Fed. Cir. 1983). As set out above, Appellant has set out what is necessary for one skilled in the art to practice the invention. Indeed, a mechanical engineer or any control systems engineer even without knowledge of real time computer systems but with the ability to understand what Appellant has set out in his application would have no problem configuring a control system by just asking those persons skilled in the real time computer system art what to properly use (even if there weren't people both skilled in the real time computer system art and in control systems for mechanical devices). Randomex, Inc. v. Scopus Corp., 849 F.2d 585, 589 (Fed. Cir. 1988).

Conclusion

Appellant's invention is a unique combination of elements resulting in a much needed means of reducing cost for operation and maintenance of spas by unique control systems. These systems were disclosed sufficiently to enable one skilled in the art to practice these inventions. The Office's rejection of Appellant's claims lacks any factual basis and is at best founded on an improper ignoring of what those skilled in the art stated. The Office did not give any useful specific guidance on how the application was deficient so that specific details known in the art might have been added but spoke only in generalities. For this and all the foregoing reasons, the Office's rejection of the specification and claims 1-12 were erroneous and should be reversed.

Please charge any additional charges with respect to this appeal, including any charges necessary for this brief to be deemed timely filed for which Appellant hereby petitions, to the deposit account number 15-0697 of David Ostfeld, P.C.

Respectfully submitted,



David M. Ostfeld
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DMO147:03/dgd

CERTIFICATE OF MAILING

SERIAL NO.: 054,581

FILED: May 27, 1987

I hereby certify that three copies of the following

APPEAL BRIEF

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Washington, D.C. 20231

on February 5, 1990.

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Feb 5, 1990
Date

DMO147:03/dgd

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APPENDIX

The claims on appeal are as follows:

1. A spa control system comprising a control panel, output components, and a heating element which heats the water in the spa, and further comprising:

a solid state sensor for detecting the temperature of water in the spa;

a solid state sensor for detecting the temperature of the heating element; and

a microcomputer for processing the signals from said sensors to calculate the temperature of the water and the heating element so that the heating element controls the temperature of the water within a prescribed range.

2. A system as described in Claim 1, further comprising a Traic which drives at least one output component of the spa control system.

3. A system as described in Claim 1, further comprising an Opto-Isolator connected between the control panel and the Traics for electrically isolating the control system from the main power supply.

4. A spa control system for detecting the malfunction of components within the system, comprising:

a display;

a pump;

a heating element;

a system interconnection panel which is connected to said pump and said heater; and

a microcomputer within said system interconnection panel for detecting the malfunction of said pump or said heating element and for generating a signal which illuminates said display to slow the

10666

malfunction of the component.

5. A spa control system for controlling the temperature of water in the spa, comprising:

a heating element for heating the water;

a solid state sensor for detecting the temperature of the water;

a solid state sensor for detecting the temperature of said heating element;

a microcomputer for processing signals generated by said sensors to compute the temperature of the water and of said heating element, wherein said microcomputer activates and deactivates said heating element to control the temperature of said water within a selected range.

6. A spa control system as described in Claim 5, wherein said microcomputer activates said heating element to heat the water to a selected temperature without heating the water above the selected temperature.

7. A spa control system as described in Claim 5, wherein said microcomputer calculates the rate of heating of the water and said heating element, and activates and deactivates said heating element to heat the water to a selected temperature.

8. A spa control system for controlling the temperature of water in a spa, comprising:

a system interconnection panel containing a microcomputer and being connected to a power supply;

a control panel connected to said system interconnection panel;

a heating element connected to said system interconnection panel; and

a pump for circulating water over said heating element.

9. A spa control system as described in Claim 8, further comprising a heat sink adjacent said water for transferring heat from said system interconnection panel to said water.

10. A spa control system as described in Claim 8, further comprising a display in said control panel for slowing certain characters calculated by said microcomputer.

11. A spa control system as described in Claim 10, wherein said display slows a character sent by said microcomputer which identifies a malfunction of said spa control system.

12. A spa control system as described in Claim 10, wherein said display indicates the operation time of selected components of the spa control system.

AJA04:35

EXHIBIT C

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 17

Serial Number: 07/054,581
Filing Date: MAY 27, 1987
Appellant(s): MICHAEL E. TOMPKINS ET AL.

DAVID M. OSTFELD
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed Feb. 8, 1990.

(1) *Status of claims.*

The statement of the status of claims contained in the brief is correct.

(2) *Status of Amendments After Final.*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(3) *Summary of invention.*

The summary of invention contained in the brief is deficient because Appellant does not give a concise explanation of the invention as defined in the claims, does not refer to the

specification by page and line number or to the drawings by reference to characters.

The following is a concise explanation of the invention:

The present invention provides for a spa control system generally comprising a heating element, a sensor for detecting the temperature of the water, and a microcomputer for processing signals generated by said sensor and for activating and deactivating the heating element. In one embodiment of the invention, the microcomputer assesses the time necessary to heat water from an initial temperature to a selected temperature. From this information, the heating rate of the water can be calculated. The heating rate can be stored by the microcomputer and can be used to determine the start time necessary to heat the spa water from an initial temperature to a selected temperature by a desired time. In another embodiment of the invention, the temperature difference between two sensors in the spa system can be monitored to detect problems in the system. (Page 2, lines 19-31).

(4) *Issues*.

The appellant's statement of the issues in the brief is substantially correct. The changes are as follows: The issue is whether or not one of ordinary skill in the art of regulating a spa would be able to make and use the invention given the Appellant's Specification.

(5) *Grouping of claims*.

The rejection of claims 1-12 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together. See 37 C.F.R.

Missing

PAGE 3

Patent Imaging Corporation

(703) 553-0000

File History Division

File History: _____ Order Date: _____

Mentioned In: _____ Filing Date: _____

_____ _____

References: ( ) Yes ( ) No

Related Applns. ( ) Yes ( ) No

RUSH ( ) Yes ( ) No

Certified: ( ) Yes ( ) No

Comments:

_____

_____

_____

_____

Status: _____

_____

_____

_____

_____

§ 1.192(c)(5).

(6) *Claims appealed.*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(7) *Prior Art of record.*

No prior art are relied upon by the examiner in the rejection of claims under appeal.

(8) *New prior art.*

No new prior art has been applied in this examiner's answer.

(9) *Grounds of rejection.*

The following ground(s) of rejection are applicable to the appealed claims.

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is mostly nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification is objected to under 35 U.S.C. § 112, first paragraph, as failing to adequately teach how to make and use the claimed invention.

To comply with the ennablement clause of the first paragraph of 35 U.S.C. 112, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. In re Scarbrough, 500 F.2d 560, 182 USPQ

298 (CCPA 1974); In re Brandstadter, 484 F.2d 1395, 179 USPQ 286 (CCPA 1973); In re Gay, 50 CCPA 725, 309 F.2d 769, 135 USPQ 311 (1962). If the examiner had a reasonable basis for questioning the sufficiency of the disclosure, the burden shifted to the Appellants to come forward with evidence to rebut this challenge. In re Doyle, 482 F.2d 985, 179 USPQ 237 (1973). The burden is placed initially upon the examiner to establish a reasonable basis for questioning the adequacy of the disclosure. In re Strahilevitz, 668 F.2d 1229, 212 USPQ 561 (CCPA 1982); In re Angstadt, 537 F.2d 676, 185 USPQ 152 (CCPA 1975).

The specification is objected to under 35 USC 112 and Rule 71 as being vague, indefinite and containing insufficient disclosure to support the appended claims. The statue imposes upon applicant for letter patent the responsibility of providing a written description of the invention in such a clear and exact terms as to enable one skilled in the art to make and use the invention.

In a block diagram disclosure of a complex claimed system which includes a microcomputer and other system components controlled by the microcomputer, a mere reference to a prior art, commercially available microcomputer, without any description of the precise operations to be performed by the microcomputer, fails to disclose how such a microcomputer would be properly programmed to either perform any required calculation - in the present arrangement the determination of PH levels, and the monitoring of temperature to determine when the heater should be engaged,

diagnostic mode - or to coordinate the other system components in the proper time sequence to perform the functions disclosed and claimed. One of ordinary skill in the art would have to rely on undue experimentation to perform the claimed invention.

It is noted that Appellant's claimed invention is a control system for control system for controlling a SPA by the use of a microcomputer or microcontroller; in another embodiment the claimed invention is a microcomputer for determining a malfunction condition and for generating a signal which illuminates the display to slow the malfunction; and, a microcomputer for activating and deactivating the heating elements. In essence Appellant's invention is an aptly programmed microcomputer which performs the function of controlling, diagnostic routines, and activating or deactivating.

The controlling a spa, performing diagnostic, and deactivating or activating are functions which are quite known to those in the art, but only manually. For example, the patent to Hancock discloses a control panel. Hancock's figures 4 and 9 shows that the control panel is electrical-mechanical. The patent to Ramseur et al. shows another electrical-mechanical SPA controller which compares the temperature of the heater (column 2, line 58) and the temperature of the water (column 3, lines 4-7). The patent to Hatcher is a remote controller for controlling the temperature of the water in the spa. The patent to Raleigh et al. is a conventional electrical-mechanical system which in addition to

regulating the temperature of the water includes a safety circuit. The patent to Castleberry et al. is a thermostat control of the heating element with a limit switch for preventing over heating. The patent to Krumhansl appears to suggest the use of a controller other than electrical-mechanical for controlling the temperature of the water in the spa (see columns 5 and 6). There is no suggestion in Krumhansl to substitute a microcomputer for a controller. The patent to Barrett, Sr. et al. is an electrical mechanical controller. The patent to Ramey which regulates the water temperature in a pool by the use of thermostats. Finally, the patent to Whitaker et al. concerns the controlling of a heat exchanger for providing hot water to a spa.

Appellant's disclosure is deficient in that it fails to teach how those in the art can program the microcomputer to determine the PH level, monitor the temperature, control the operation of activating and deactivating at the required period, and the performing diagnostic routines.

Appellant states the following concerning the programming of the computer:

> The Analog Conversion Program manipulates the converter circuitry to convert sensor input signals to digital information. This program also converts the digital information to engineering units for the purpose of display and comparison. The RTC control program controls all interaction with the Real Time Clock. The program is responsible for loading data for future events. The PID Control stands for proportional, integral and derivative. This program monitors the temperature of the water and determines when the heater should be engaged. The program issues a command which activates the heater and then monitors the temperature to determine when the heater should be turned

> off. The program is unique that it monitors the rate decrease and the rate of increase of water temperature so that the final temperature of the water is not higher or lower than the selected temperature. The spa control system can achieve an accuracy of plus or minus one degree fahrenheit with the heating and monitoring elements.
>
> The output control program issues commands to the output components to turn on the TRIACS for control of the pump, heater, blower, lights and other components. The input scanning program monitors devices such as push buttons and switches. The flow switch would be monitored by this program, as well as any other shut down or feed back signals. The PH algorithm converts raw digital data received from the A-D converter on the PH channel and converts this data to standard PH units of measure. (Cited with emphasis pages 6-7).

Appellant's disclosure enumerates all the function performed by the program (see emphasized section above). Appellant has made no reference to known programs to perform all the above tasks. Appellant has not provided a flowchart nor has Appellant detailed the operations that should be taken by the programmer. Appellant simply heralds the virtues of this computer program and expects those in the art to fill in the gaps. The latitude of the gaps are simple too great to enable one of ordinary skill in the art to make and use the invention given the rudimentary knowledge of computers, if at all, on the spa art.

The art of record reveals (a) the state of the prior art; and, (b) the relative skill in the prior art. As can be seen from the art of record there is support for performing temperature control in the spa art. The prior art does not, however, show a computer. The issue is not that a computer is not known in the art, but rather how one can program a computer to perform the above tasks. The art merely demonstrates a rudimentary knowledge of computers

(see patent to Krumhansi).

The skill of those in the art appears to be mainly in the electrical-mechanical area of controlling a spa. The patent to Kurmhansl indicate that knowledge of computers, microprocessors, or microcontrollers was nascent in 1986. The claimed invention represents an introduction to the computer age, and, as such, it is important for the application to increase the knowledge of those of ordinary skill in the art by supplying publication or patents which disclose these features or teach in detail these features (see In re Ghiron, 169 USPQ 723 (1971)).

(10) *New ground of rejection.*

This Examiner's Answer does not contain any new ground of rejection.

(11) *Response to argument.*

The procedure posture is that the Examiner has advanced a reasonable basis for questioning the adequacy of the disclosure and it was incumbent upon Applicant to rebut the challenge. See In re Doyle, 179 USPQ 237 (1973).

The Examiner having met the initial burden [1], the Appellant attempted to rebut the challenge by asserting that he could make and use the invention as disclosed. Thus, the ultimate issue to be discussed is whether or not Appellant's representative statements

[1] Appellant admitted in the communication filed on Nov. 30, 1988 that "(w)hat is important is the algorithms being used in the microcomputer and how they operate." Appellant's statement is taken to mean that he too considers the computer program important to practice his invention.

can be used to rebut the challenge made by the Examiner that the invention is not adequately disclosed.

Arguments by counsel may be effective in establishing that an Examiner has not properly met his burden or erred in his position. It is well settled, however, that argument of counsel alone cannot take place of evidence in the record once the Examiner has advanced a reasonable basis for questioning the disclosure. See In re Budnick, 190 USPQ 422 (CCPA 1976).

The record indicates that counsel has from the beginning argued that he has the necessary skills to make and use the invention as discussed. In the brief, Appellant makes the same arguments. Further, Appellant did not explicitly challenge the adequacy of the Examiner's basis, Appellant has only offered the opinion, standing alone, that he could make and use the invention as disclosed. The 35 USC section 112 should be sustained on this ground.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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PATENT EXAMINER
GROUP 2300

JACK B. HARVEY
SUPERVISORY PATENT EXAMINER
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ER/hh
July 2, 1993

978

DEADLINE POSTED

10493

Date: 8/12/93

Action: Response To Examiner's Answer Due

Attorneys: DMO

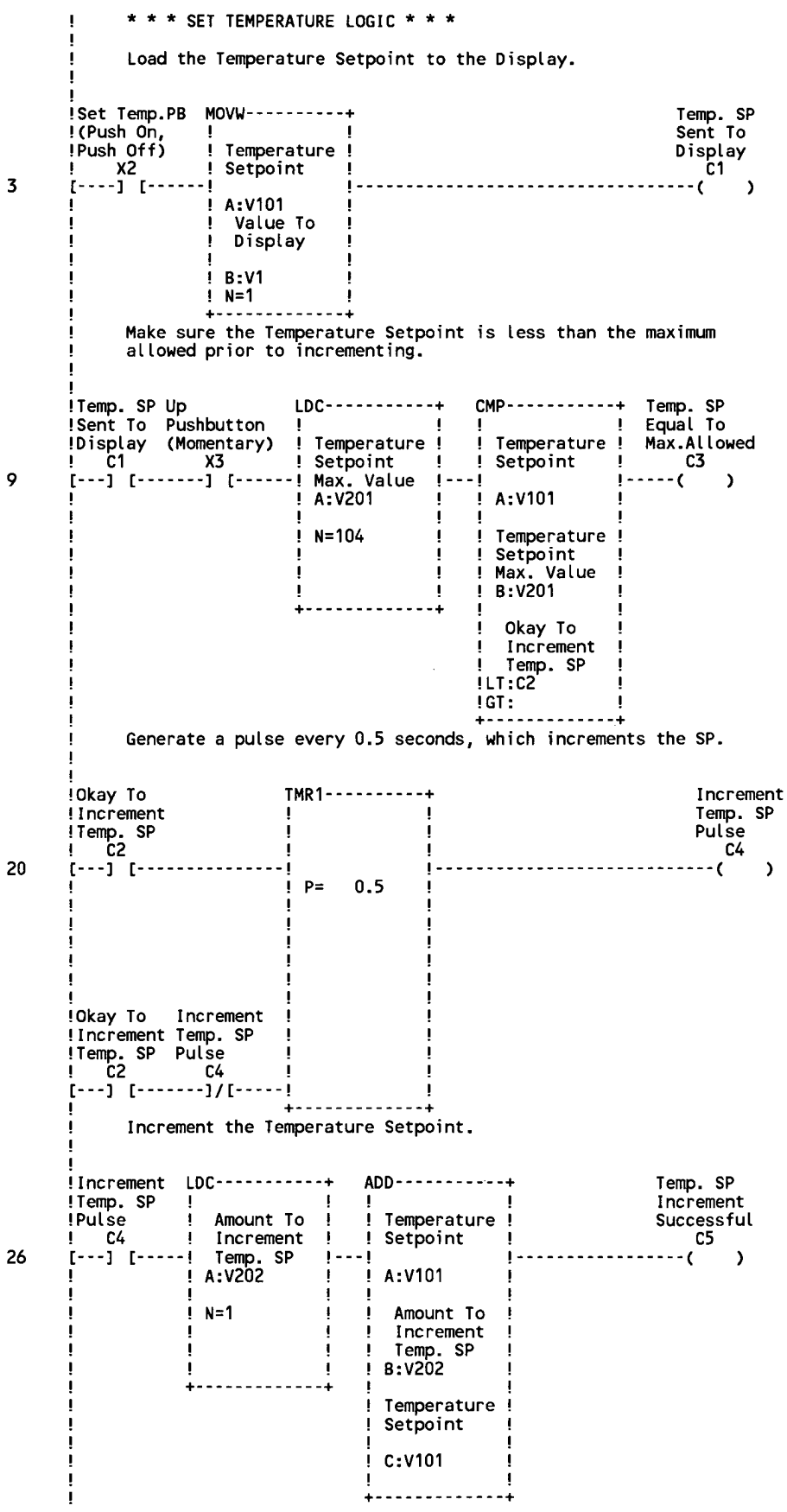
Siegel, Chip
Client Name

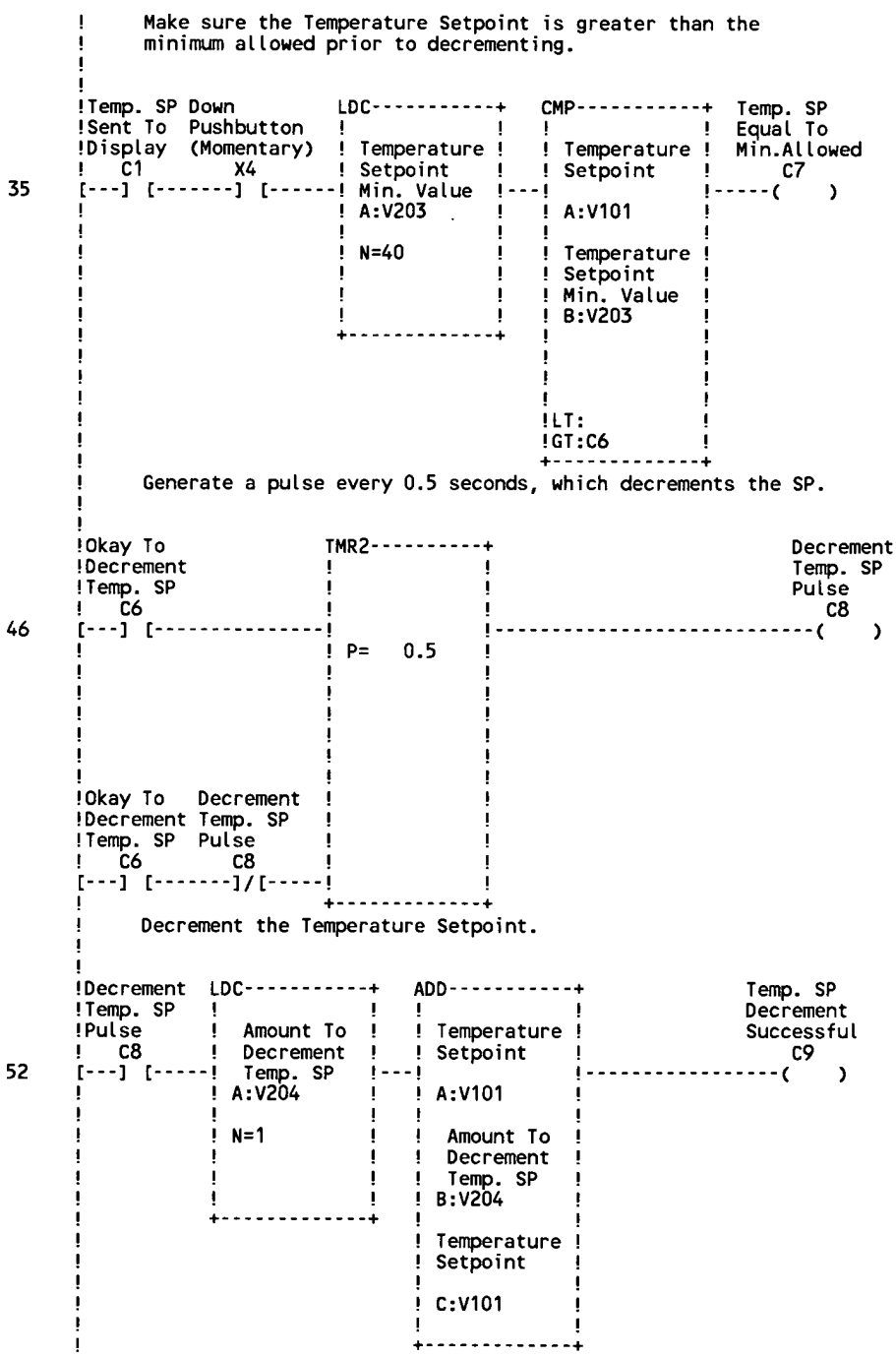
86-1198-01
Client Number

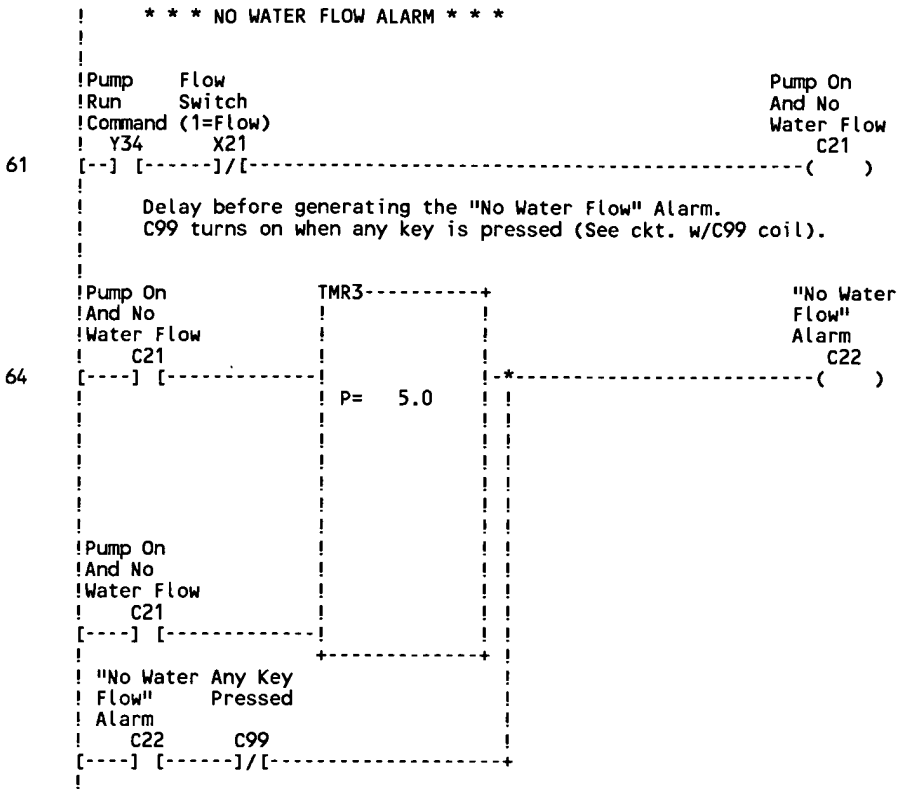
553

EXHIBIT D

```
     !     * * * BLOWER LOGIC * * *
     !
     !
     !Blower PB                                                  Blower
     !(Push On,                                                 Run
     !Push Off)                                                 Command
     !   X1                                                       Y33
1    [---] [-----------------------------------------------------(    )
     !
```


* * * SET TEMPERATURE LOGIC * * *
Load the Temperature Setpoint to the Display.
Set Temp.PB (Push On, Push Off) X2
MOVW
Temperature Setpoint
A:V101 Value To Display
B:V1 N=1
Temp. SP Sent To Display C1
3
Make sure the Temperature Setpoint is less than the maximum allowed prior to incrementing.
Temp. SP Up Sent To Display C1 Pushbutton (Momentary) X3
LDC
Temperature Setpoint Max. Value
A:V201 N=104
CMP
Temperature Setpoint Max. Value
A:V101 B:V201
Okay To Increment Temp. SP
LT:C2 GT:
Temp. SP Equal To Max.Allowed C3
9
Generate a pulse every 0.5 seconds, which increments the SP.
Okay To Increment Temp. SP C2
TMR1
P= 0.5
Increment Temp. SP Pulse C4
20
Okay To Increment Temp. SP C2 Increment Temp. SP Pulse C4
Increment the Temperature Setpoint.
Increment Temp. SP Pulse C4
LDC
Amount To Increment Temp. SP
A:V202 N=1
ADD
Temperature Setpoint
A:V101
Amount To Increment Temp. SP
B:V202
Temperature Setpoint
C:V101
Temp. SP Increment Successful C5
26


Make sure the Temperature Setpoint is greater than the minimum allowed prior to decrementing.
Temp. SP Down Sent To Display C1
Pushbutton (Momentary) X4
LDC
Temperature Setpoint Min. Value
A:V203
N=40
CMP
Temperature Setpoint
A:V101
Temperature Setpoint Min. Value
B:V203
LT:
GT:C6
Temp. SP Equal To Min.Allowed C7
35
Generate a pulse every 0.5 seconds, which decrements the SP.
Okay To Decrement Temp. SP C6
TMR2
P= 0.5
Decrement Temp. SP Pulse C8
46
Okay To Decrement Temp. SP C6
Decrement Temp. SP Pulse C8
Decrement the Temperature Setpoint.
Decrement Temp. SP Pulse C8
LDC
Amount To Decrement Temp. SP
A:V204
N=1
ADD
Temperature Setpoint
A:V101
Amount To Decrement Temp. SP
B:V204
Temperature Setpoint
C:V101
Temp. SP Decrement Successful C9
52


* * * NO WATER FLOW ALARM * * *
Pump Run Command (1=Flow)
Flow Switch
Y34
X21
Pump On And No Water Flow
C21
61
Delay before generating the "No Water Flow" Alarm.
C99 turns on when any key is pressed (See ckt. w/C99 coil).
Pump On And No Water Flow
C21
TMR3
P= 5.0
"No Water Flow" Alarm
C22
64
Pump On And No Water Flow
C21
"No Water Flow" Alarm
C22
Any Key Pressed
C99

OKI semiconductor

MSM5832RS

REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

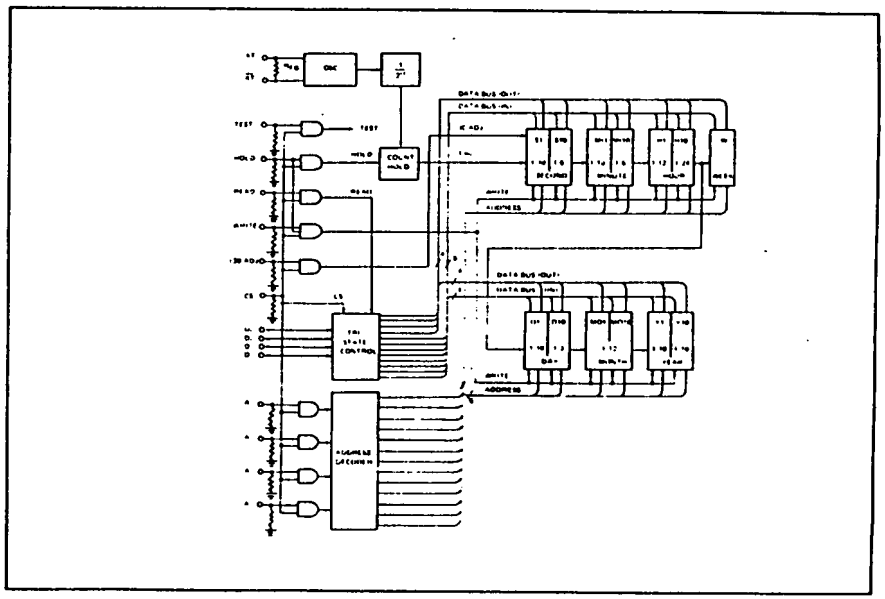
The MSM5832RS is a metal-gate CMOS Real Time Clock/Calendar for use in bus-oriented microprocessor applications. The on-chip 32.768Hz crystal controlled oscillator time base is divided to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ±30 second correction.

The MSM5832RS normally operates from a 5V ±5% supply. Battery backup operation down to 2.2V allows continuation of time keeping when main power is off. The MSM5832RS is offered in an 18-lead dual-in-line plastic (RS suffix) package.

FEATURES

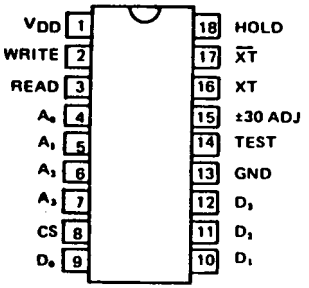
- 7 Function – SECOND, MINUTE, HOUR, DAY, DAY-OF-WEEK, MONTH, YEAR
- Automatic leap year calendar
- 12 or 24 hour format
- ±30 second error correction
- 4-BIT DATA BUS
- 4-BIT ADDRESS
- READ, WRITE, HOLD, and CHIP SELECT Inputs
- Reference signal outputs – 1024, 1, 1/60, 1/3600Hz
- 32.768kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to V_{DD} = 2.2V
- Low power dissipation
  90 μW Max. at V_{DD} = 3V
  2.5 mW Max. at V_{DD} = 5V
- 18 pin plastic DIP package

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

A0 to A3	:	Address Inputs.
WRITE	:	Write Enable
READ	:	Read Enable
HOLD	:	Count Hold
CS	:	Chip Select
D0 to D3	:	Data Input Output
TEST	:	Test Input
±30 ADJ	:	±30 Second Correction Input
XT & $\overline{XT}$	:	xtal oscillator connections
V_{DD}	:	+5V Supply
GND	:	Ground



REGISTER TABLE

Address Input				Register Name	Data Input/Output				Data Limit	Remarks
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S1	•	•	•	•	0 ~ 9	S1 or S10 are reset to zero irrespective of input data D0–D3 when write instruction is executed with address selection.
1	0	0	0	S10	•	•	•		0 ~ 5	
0	1	0	0	MI1	•	•	•	•	0 ~ 9	
1	1	0	0	MI10	•	•	•		0 ~ 5	
0	0	1	0	H1	•	•	•	•	0 ~ 9	
1	0	1	0	H10	•	•	†	†	0 ~ 1 / 0~2	D2 = "1" for PM D3 = "1" for 24 hour format D2 = "0" for AM D3 = "0" for 12 hour format
0	1	1	0	W	•	•	•		0 ~ 6	
1	1	1	0	D1	•	•	•	•	0 ~ 9	
0	0	0	1	D10	•	•	†		0 ~ 3	D2 = "1" for 29 days in month 2 (2) D2 = "0" for 28 days in month 2
1	0	0	1	MO1	•	•	•	•	0 ~ 9	
1	1	0	1	MO2	-	-	-	-	0 ~ 9	
0	1	0	1	MO10	•				0 ~ 1	
1	1	0	1	Y1	•	•	•	•	0 ~ 9	
0	0	1	1	Y10	•	•	•	•	0 ~ 9	

(1) •data valid as "0" or "1".
Blank does not exist (unrecognized during a write and held at "0" during a read)
†data bits used for AM/PM, 12/24 HOUR and leap year.

(2) If D2 previously set to "1", upon completion of month 2 day 29, D2 will be internally reset to "0".

OSCILLATOR FREQUENCY DEVIATIONS

Frequency Deviation vs Temperature

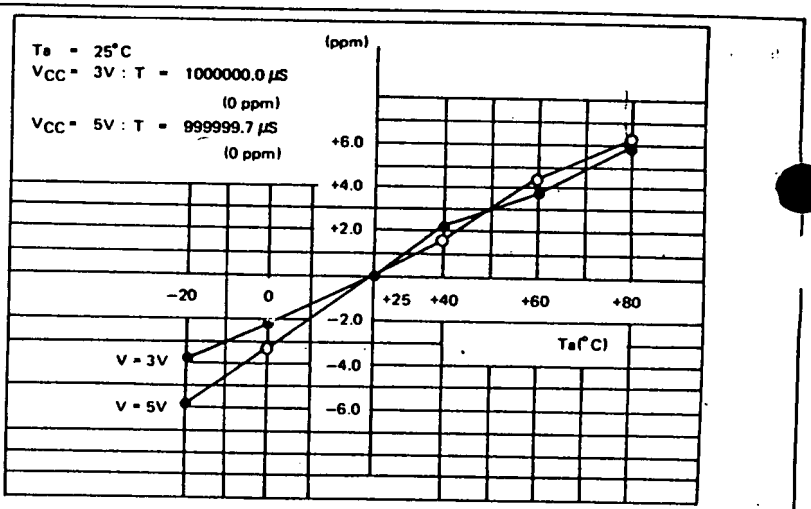


Figure 1

Frequency Deviation vs Supply Voltage

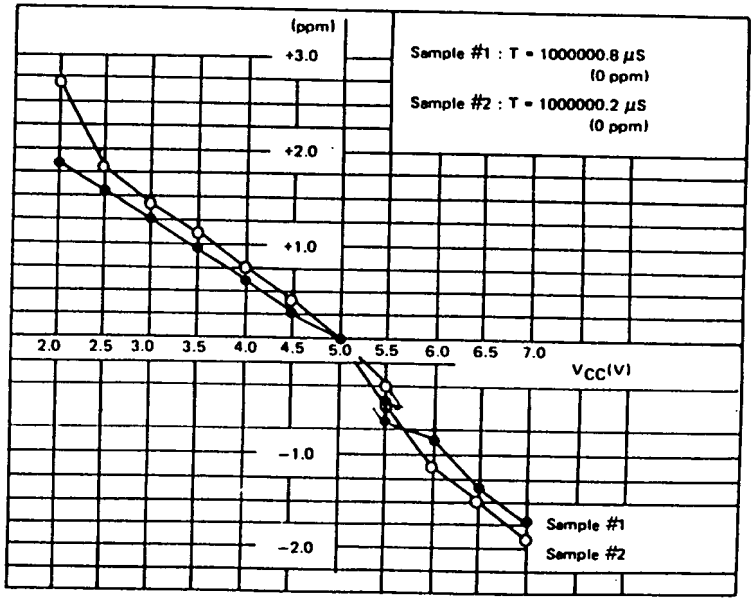


Figure 2

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD} + 0.3	V
Data I/O voltage	$V_{\overline{O}}$	−0.3 ~ V_{DD} + 0.3	V
Storage Temperature	Tstg	−55 ~ 150	°C

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	4.5	5	7	V	
Standby Supply Voltage	V_{DH}	2.2	–	7	V	
Input Signal Level	V_{IH}	3.6	–	V_{DD}	V	V_{DD} = 5V ± 5% Respect to GND
	V_{IL}	−0.3	–	0.8	V	
Crystal Oscillator Freq.	f(XT)	–	32.768	–	kHz	
Operating Temperature	T_{OP}	−30	–	+85	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ±5%; T_A = −30 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I_{IH}	10	25	50	μA	V_{IN}=5V, V_{DD}=5V
	I_{IL}	–	–	-1	μA	V_{IN} = 0V
Data I/O Leakage Current	I_{LD}	-10	–	10	μA	$V_{I/O}$ = 0 to V_{DD} CS = "0"
Output Low Voltage	V_{OL}	–	–	0.4	V	I_O = 1.6 mA, CS = "1", READ = "1"
Output Low Current	I_{OL}	1.6	–	–	mA	V_O = 0.4V, CS = "1", READ = "1"
Operating Supply Current	I_{DDS}	–	15	30	μA	V_{CC} = 3V, Ta = 25°C
	I_{DD}	–	100	500	μA	V_{CC} = 5V, Ta = 25°C

(1) XT, $\overline{XT}$ and D_0 ~ D_3 excluded.

SWITCHING CHARACTERISTICS

(1) READ mode

(V_{DD} = 5V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	——	150	–	–	μs
HOLD Hold Time	t_{HH}	——	0	–	–	μs
HOLD Pulse Width	t_{HW}	——	–	–	990	ms
HOLD "L" Hold Time	t_{HL}	——	130	–	–	μs
READ Hold Time	t_{RH}	——	0	–	–	μs
READ Set-up Time	t_{RS}	——	0	–	–	μs
READ Access Time	t_{RA}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	–	–	6	μs
ADDRESS Set-up Time	t_{AS}	——	3	–	–	μs
ADDRESS Hold Time	t_{AH}	——	0.2	–	–	μs
READ Pulse Width	t_{RW}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	2	–	–	μs
DARA Access Time	t_{AC}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	–	–	0.6	μs
OUTPUT Disable Time	t_{OFF}	$R_{PULL-UP}$ = 5KΩ C_L = 15 pF	–	–	0.6	μs
CS Enable Delay Time	t_{CS1}	——	–	–	0.6	μs
CS Disable Delay Time	t_{CS2}	——	–	–	0.6	μs

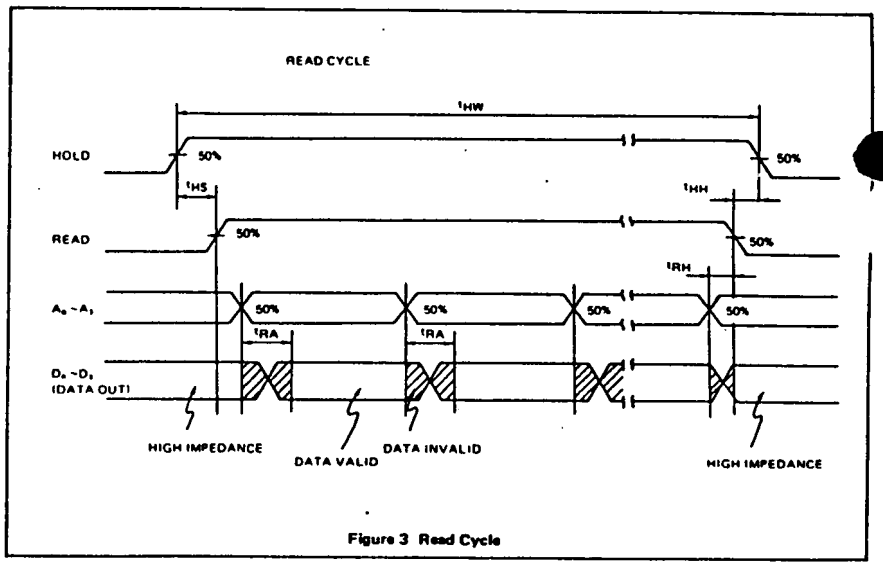


Figure 3 Read Cycle

Notes: 1. A Read occurs during the overlap of a high CS and a high READ.
2. CS may be a permanent "1", or may be coincident with HOLD pulse.

SWITCHING CHARACTERISTICS

(2) WRITE mode

(V_{DD} = 5V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	——	150	–	–	μs
HOLD Bold Time	t_{HH}	——	0	–	–	μs
HOLD Pulse Width	t_{HW}	——	–	–	990	ms
HOLD "L" Hold Time	t_{HL}	——	130	–	–	μs
ADDRESS Pulse Width	t_{AW}	——	1.7	–	–	μs
Data Pulse Width	t_{DW}	——	1.7	–	–	μs
DATA Set-up Time	t_{DS}	——	0.5	–	–	μs
DATA Hold Time	t_{DH}	——	0.2	–	–	μs
WRITE Pulse Width	t_{WW}	——	1.0	–	–	μs
CS Enable Delay Time	t_{CS1}	——	–	–	0.6	μs
CS Disable Delay Time	t_{CS2}	——	–	–	0.6	μs

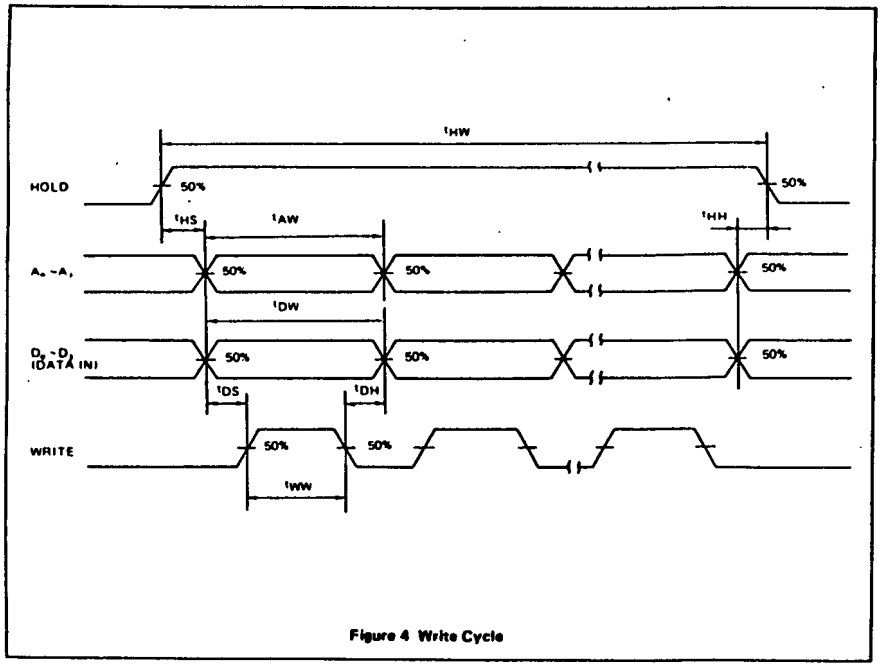


Figure 4 Write Cycle

Notes: 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE.
2. CS may be permanent "1", or may be coincident with HOLD pulse.

PIN DESCRIPTION

Name	Pin No.	Description
V_{DD}	1	Power supply pin. Application circuits for power supply are described in Figure 9.
WRITE	2	Data write pin. Data write cycle is described in Figure 4.
READ	3	Data read pin. Data read cycle is described in Figure 3.
$A_0 \sim A_3$	4 ~ 7	Address input pins used to select internal counters for read/write operations. The address is specified by 4-bit binary code as shown in Table 1.
C S	8	Chip slect pin which is required to interface with the external circuit. HOLD, WRITE, READ, ±30ADJ, TEST, $D_0 \sim D_3$ and $A_0 \sim A_3$ pins are activated if CS is set at H level, while all of these pins are disabled if CS is set at L level.
$D_0 \sim D_3$	9 ~ 12	Data input/output pins (bidirectional bus). As shown in Figure 5, external pull-up registers of 4.7 kΩ ~ 10 kΩ are required by the open-drain NMOS output. D_3 is the MSB, while D_0 is the LSB

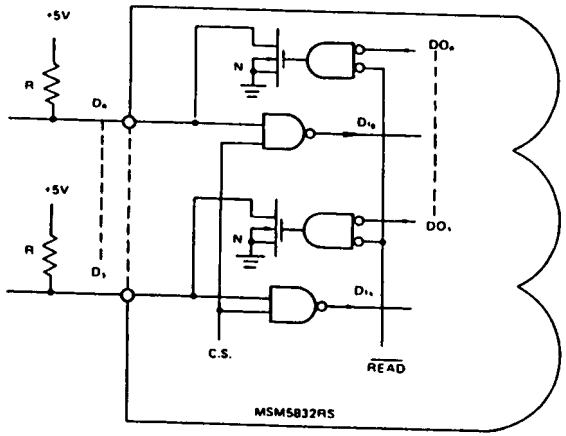


Figure 5

Name	Pin No.	Description
GND	13	Ground pin.
TEST	14	Test pin. Normally this pin should be left open or should be set at ground level. With CS at V_{DD}, pulses to V_{DD} on the TEST input will directly clock the S_1, MI_{10}, W, D_1 and Y_1 counters, depending on which counter is addressed (W and D_1 are selected by D_1 address in this mode only). Roll-over to next counter is enabled in this mode.
±30ADJ	15	This pin is used to adjust the time within the extent of ± 30 seconds. If this pin is set at H level when the seconds digits are 0 ~ 29, the seconds digits are cleared to 0. If this pin is set at H level when the seconds digits are 30 ~ 59, the second digits will be cleared to 0 and the minutes digits will be increased by +1. To enable this function, 31.25 ms or more width's pulse should be input to this pin.
XT	16	Oscillator pin. 32.768 kHz crystal, capacitor and trimmer condensor for frequency adjustment connected to these pins. See Figure 6. As for oscillator frequency deviation, refer to Figure 1 and Figure 2. If an external clock is to be used for the MSM5832RS's oscillation source, the external clock is to be input to XT, and $\overline{XT}$ should be left open.
$\overline{XT}$	17	
HOLD	18	Switching this input to V_{DD} inhibits the internal 1 Hz clock to the S1 counter. After the specified HOLD set-up time (150 μs), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 990 ms, real time accuracy will be undisturbed. Pull-down to GND is provided by an internal resistor.

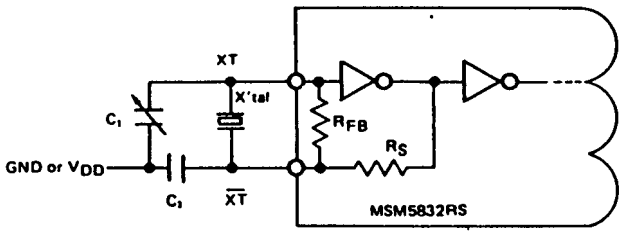


Figure 6

REFERENCE SIGNAL OUTPUT PIN

Condition	Output	Reference Frequency	Pulse Width
HOLD = L	D_0 (1)	1024 Hz	duty 50%
READ = H	D_1	1 Hz	122.1 μS
CS = H	D_2	1/60 Hz	122.1 μS
$A_0 \sim A_2$ = H	D_3	1/3600 Hz	122.1 μS

(1) 1024 Hz signal at D_0 not dependent on HOLD input level.

APPLICATION EXAMPLE

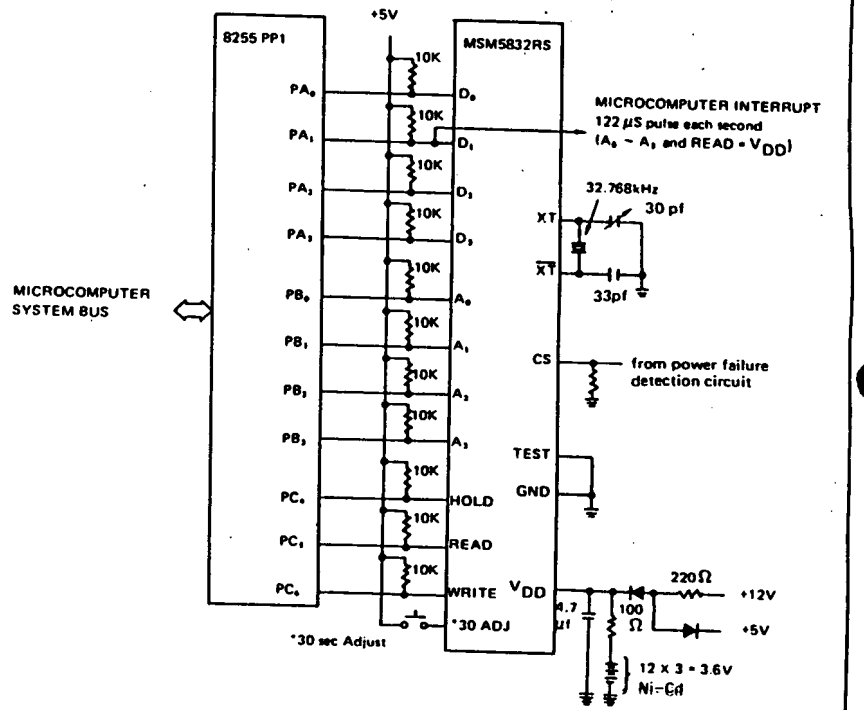


Figure 7

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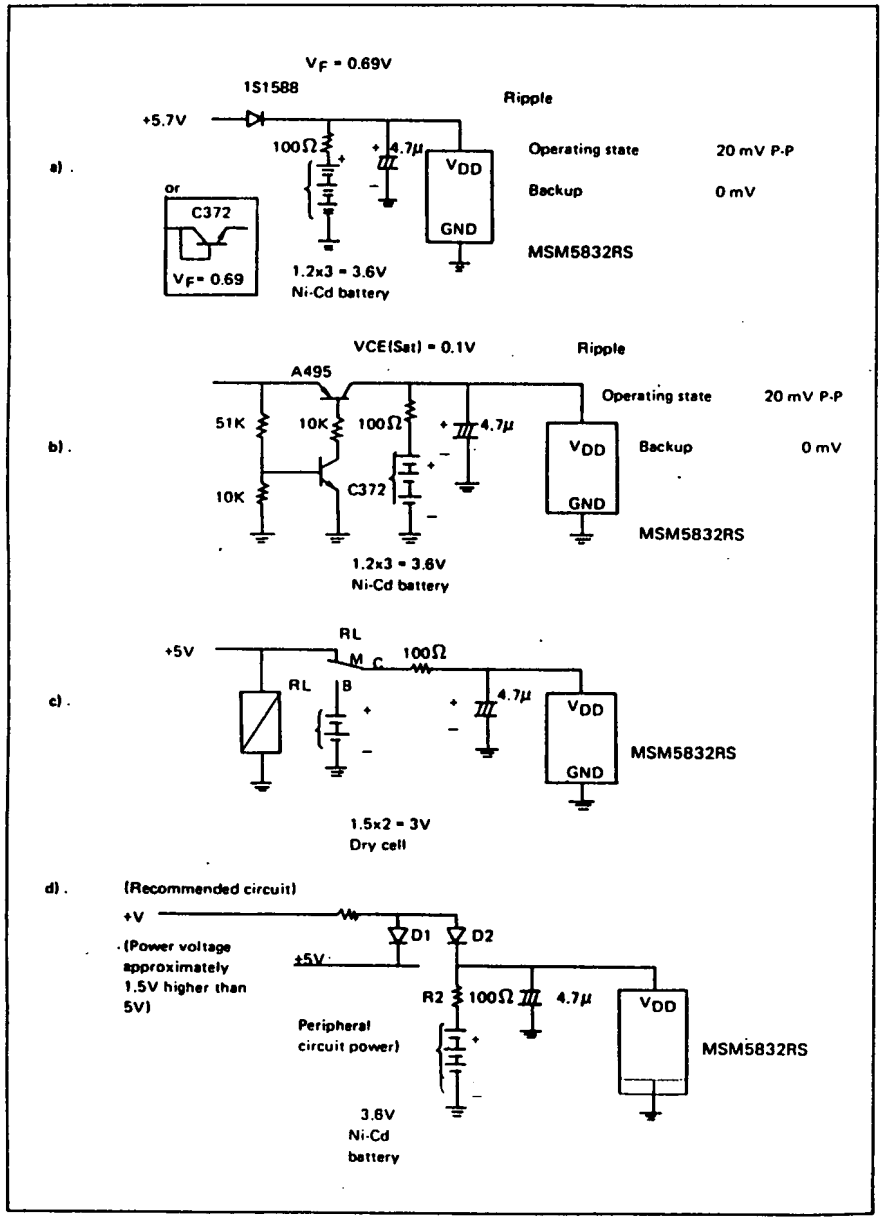
APPLICATION CIRCUIT – POWER SUPPLY CIRCUIT

Open or ground unused pins (pins other than the XT, $\overline{XT}$, D0–D3, and $\overline{BUSY}$ pins).



Note: Use the same diodes for D1 and D2 to reduce the level difference between +5V and V_{DD} of the MSM5832RS.

OKI semiconductor

MSM58321RS

REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM58321RS is a metal gate CMOS Real Time Clock/Calendar with a battery backup function for use in bus-oriented microprocessor applications.

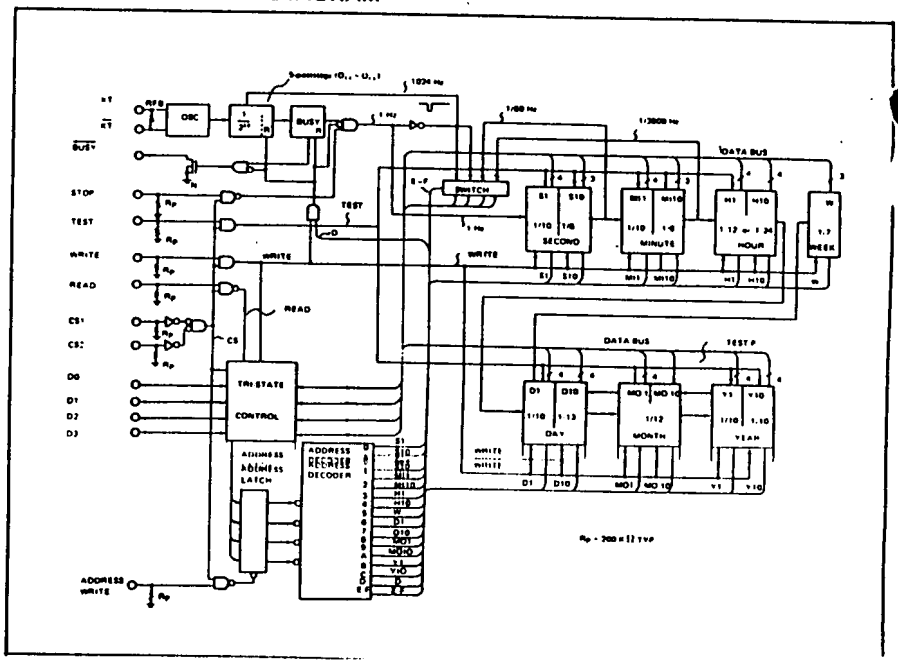
The 4-bit bidirectional bus line method is used for the data I/O circuit; the clock is set, corrected, or read by accessing the memory.

The time is read with 4-bit DATA I/O, ADDRESS WRITE, READ, and $\overline{BUSY}$; it is written with 4-bit DATA I/O, ADDRESS WRITE, WRITE, and $\overline{BUSY}$.

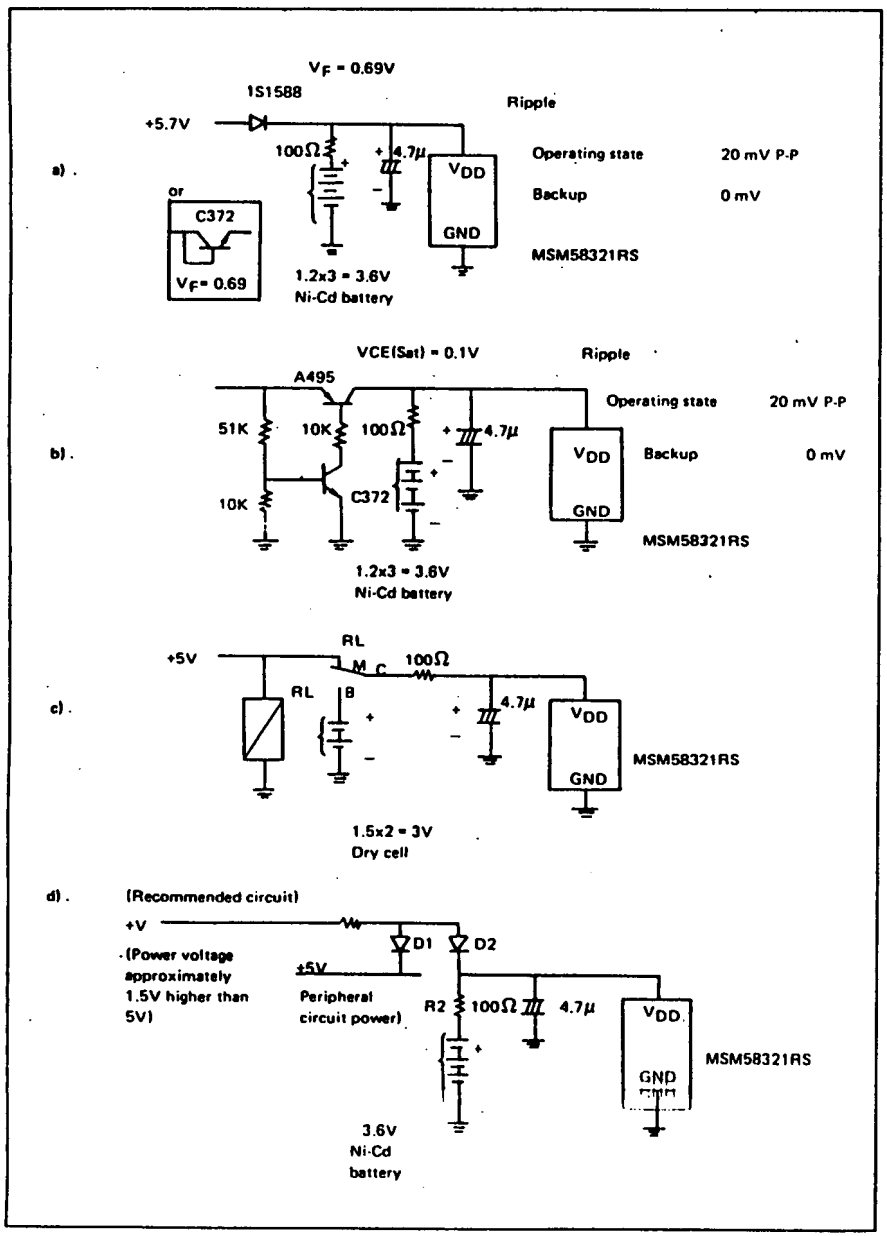
FEATURES

- 7 Function-Second, Minute, Hour, Day, Day-of-Week, Month, Year
- Automatic leap year calender
- 12/24 hour format
- Frequency divider 5-poststage reset
- Reference signal output
- 32.768kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to V_{DD} = 2.2V
- Low power dissipation
  90μW max. at V_{DD} = 3V
  2.5mW max. at V_{DD} = 5V
- 16 pin plastic DIP package

FUNCTIONAL BLOCK DIAGRAM



APPLICATION EXAMPLE - POWER SUPPLY CIRCUIT



OKI semiconductor

MSM6242BRS/GS-VK/JS

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM6242B is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microprocessor/Microcomputer applications. An on-chip 32.768KHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS0}$, CS1), $\overline{WRITE}$, $\overline{READ}$, and ALE. Control Registers D, E and F provide for 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the ITRPT/STND (INTERRUPT/STANDARD) Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The MSM6242B can operate in a 12/24 hour format and Leap Year timing is automatic.

The MSM6242B normally operates from a 5V ± 10% supply at −30 to 85° C. Battery backup operation down to 2.0V allows continuation of time keeping when main power is off. The MSM6242B is offered in a 18-pin plastic DIP, a 24-pin FLAT package, and a 18-pin PLCC package.

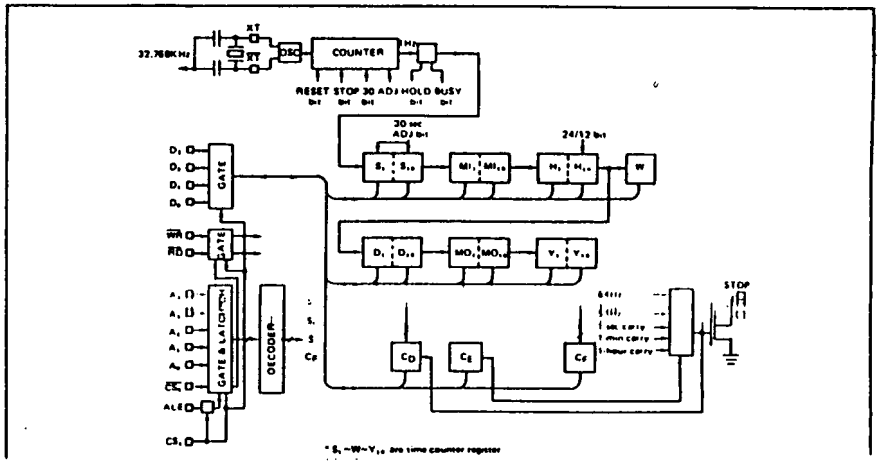
FEATURES

DIRECT MICROPROCESSOR/MICROCONTROLLER BUS CONNECTION

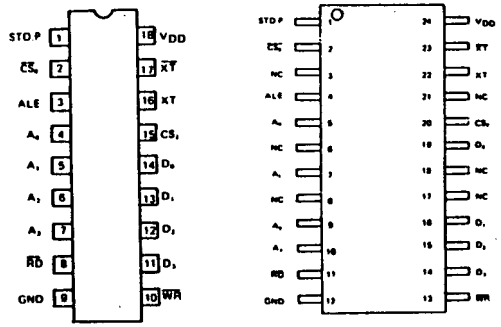
TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	80	7

- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$, ALE and CHIP SELECT INPUTS
- Status registers — IRQ and BUSY
- Selectable interrupt outputs — 1/64 second, 1 second, 1 minute, 1 hour
- Interrupt masking
- 32.768KHz crystal controlled operation
- 12/24 hour format
- Auto leap year
- ±30 second error correction
- Single 5V supply
- Battery backup down to V_{DD} = 2.0V
- Low power dissipation:
  20 μW max at V_{DD} = 2V
  150 μW max at V_{DD} = 5V
- 18-pin plastic DIP, 24-pin FLAT and 18-pin PLCC package

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



18 pin Plastic DIP Package

24 pin Plastic Flat Package

A0-A3:	Address input
D0-D3:	Data input/output
$\overline{CS0}$, $\overline{CS1}$	CHIP SELECTS 0, 1
$\overline{RD}$:	READ enable
$\overline{WR}$:	WRITE enable
ALE:	Address latch enable
STD.P:	Standard pulse output
XT, $\overline{XT}$:	XTAL oscillator input/output
VDD:	+5V supply
VSS:	ground

REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count value	Description
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 ~ 9	1-second digit register
1	0	0	0	1	S_{10}	*	S_{40}	S_{20}	S_{10}	0 ~ 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 ~ 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 ~ 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 ~ 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/AM	h_{20}	h_{10}	0 ~ 2 or 0 ~ 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 ~ 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 ~ 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 ~ 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 ~ 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 ~ 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 ~ 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 ~ 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	–	Control Register D
E	1	1	1	0	C_E	t_1	t_0	ITRPT /STND	MASK	–	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST		Control Register F

REST = RESET
ITRPT/STND = INTERRUPT/STANDARD

Note 1) – Bit * does not exist (unrecognized during a write and held at "0" during a read).
Note 2) – Be sure to mask the AM/PM bit when processing 10's of hour's data.
Bl... The IRQ FLAG bit can only be set to a "0". Setting the IRQ FLAG to a "1" is

OSCILLATOR FREQUENCY DEVIATIONS

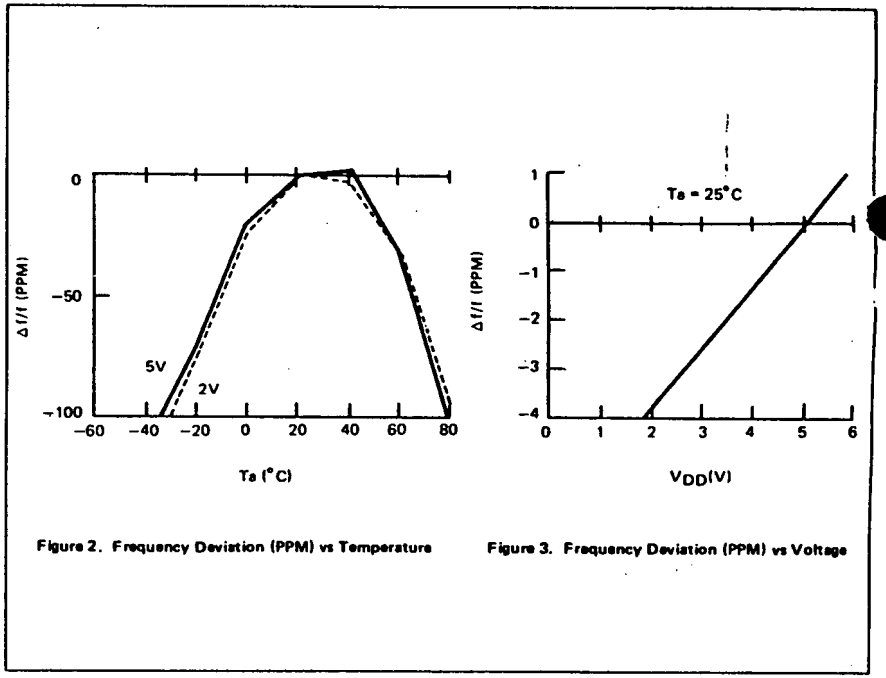
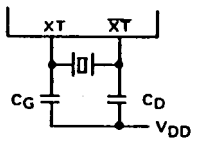


Figure 2. Frequency Deviation (PPM) vs Temperature

Figure 3. Frequency Deviation (PPM) vs Voltage

Note: 1. The graphs above showing frequency deviation vs temperature/voltage are primarily characteristic of the MSM6242B with the oscillation circuit described below.



Crystal: Type N_8, P_3 by kinseki (32.768 KHz)

C_G, C_D: 22pF (Temperature Characteristics: 0)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3~ 7	V
Input Voltage	V_I		GND − 0.3~V_{DD} + 0.3	V
Output Voltage	V_O		GND − 0.3~V_{DD} + 0.3	V
Storage Temperature	T_{STG}		−55~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	–	4 ~ 6	V
Standby Supply Voltage	V_{BAK}	–	2 ~ 6	V
Crystal Frequency	f(XT)	–	32.768	kHz
Operating Temperature	T_{OP}	–	−30~+85	°C

D.C. CHARACTERISTICS

V_{DD} = 5V ± 10%, T_A = −30 ~ +85

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage	$V_{IH}1$	–	2.2	–	–	V	All input terminals except CS_1
"L" Input Voltage	$V_{IL}1$	–	–	–	0.8		
Input Leak Current	$I_{LK}1$	V_I = V_{DD}/0V	–	–	1/−1	μA	Input terminals other than D_0 ~ D_3
Input Leak Current	$I_{LK}2$		–	–	10/−10		D_0 ~ D_3
"L" Output Voltage	$V_{OL}1$	I_{OL} = 2.5mA	–	–	0.4	V	D_0 ~ D_3
"H" Output Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–		
"L" Output Voltage	$V_{OL}2$	I_{OL} = 2.6mA	–	–	0.4	V	STD.P
OFF Leak Current	I_{OFFLK}	V = V_{DD}/0V	–	–	10	μA	
Input Capacitance	C_I	Input frequency 1MHz	–	5	–	PF	All input terminals
Current Consumption	$I_{DD}1$	f(xt) = 32.768 KHz, Ta=25°C, V_{DD} = 5V	–	–	30	μA	V_{DD}
Current Consumption	$I_{DD}2$	f(xt) = 32.768 KHz, Ta=25°C, V_{DD} = 2V	–	–	10		
"H" Input Voltage	$V_{IH}2$	V_{DD} = 2~5.5V	4/5V_{DD}	–	–	V	CS_1
"L" Input Voltage	$V_{IL}2$		–	–	1/5V_{DD}		

SWITCHING CHARACTERISTICS

(1) WRITE mode (ALE = V_{DD})

(V_{DD} = 5V ± 10% = Ta = −30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before WRITE	t_{AW}	–	20	–	
Address Stable After WRITE	t_{WA}	–	10	–	
WRITE Pulse Width	t_{WW}	–	120	–	
Data Set up Time	t_{DS}	–	100	–	
Data Hold Time	t_{DH}	–	10	–	

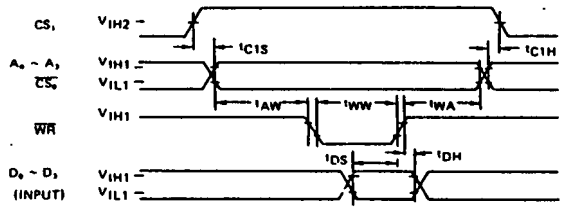


Figure 4. Write Cycle – (ALE = VDD)

(2) WRITE mode (With use of ALE)

(V_{DD} = 5 V ± 10%, Ta = −3C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{CIS}	–	1000	–	ns
Address Set up Time	t_{AS}	–	25	–	
Address Hold Time	t_{AH}	–	25	–	
ALE Pulse Width	t_{AW}	–	40	–	
ALE Before WRITE	t_{ALW}	–	10	–	
WRITE Pulse Width	t_{WW}	–	120	–	
ALE After WRITE	t_{WAL}	–	20	–	
DATA Set up Time	t_{DS}	–	100	–	
DATA Hold Time	t_{DH}	–	10	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

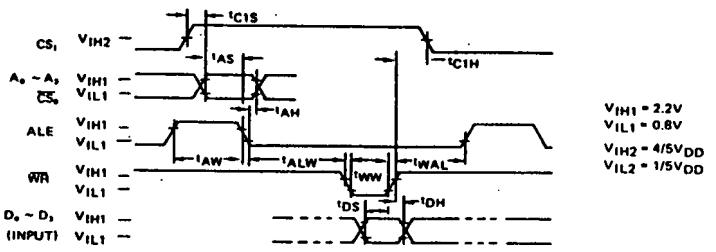


Figure 5. Write Cycle – (With Use of ALE)

(3) READ mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before READ	t_{AR}	–	20	–	
Address Stable After READ	t_{RA}	–	0	–	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	–	120	
Data Hold	t_{DR}	–	0	–	

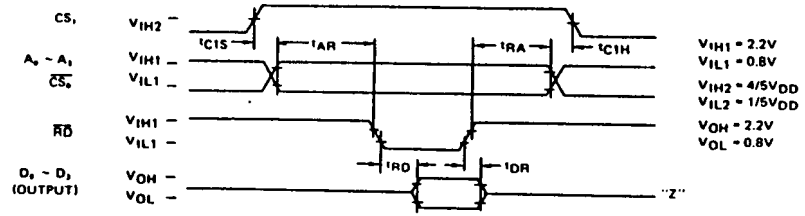


Figure 6. Read Cycle – (ALE = VDD)

(4) READ mode (With use of ALE)

(V_{DD} = 5V ±10%, Ta = –30~+85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
Address Set up Time	t_{AS}	–	25	–	
Address Hold Time	t_{AH}	–	25	–	
ALE Pulse Width	t_{AW}	–	40	–	
ALE Before READ	t_{ALR}	–	10	–	
ALE after READ	t_{RAL}	–	10	–	
RD to Data	t_{RD}	C_L = 150pF	–	120	
DATA Hold	t_{DR}	–	0	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

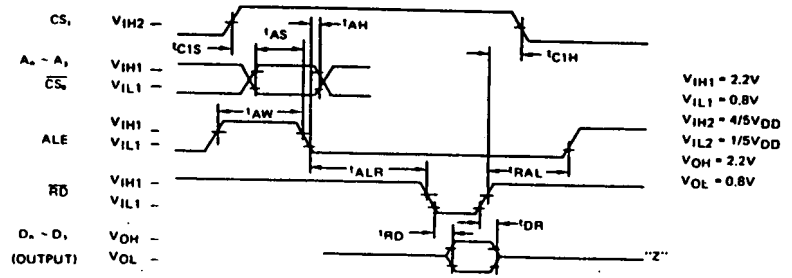
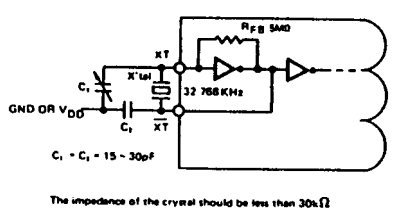


Figure 7. Read Cycle – (With Use of ALE)

PIN DESCRIPTION

Name	Pin No. RS	Pin No. GS	Description
D_0	14	19	Data Input/Output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers. D0 = LSB and D3 = MSB.
D_1	13	16	
D_2	12	15	
D_3	11	14	
A_0	4	5	Address input pin for use by a microcomputer to select internal clock/calendar's registers and control registers for Read/Write operations (See Function Table Figure 1). Address input pins A0-A3 are used in combination with ALE for addressing registers.
A_1	5	7	
A_2	6	9	
A_3	7	10	
ALE	3	4	Address Latch Enable pin. This pin enables writing of address data when ALE = 1 and $\overline{CS_0}$ = 0; address data is latched when ALE = 0 Microcontroller/Microprocessors having an ALE output should connect to this pin; otherwise it should be connected at V_{DD}.
$\overline{WR}$	10	13	Writing of data is performed by this pin. When CS_1 = 1 and $\overline{CS_0}$ = 0, $D_0 \sim D_3$ data is written into the register at the rising edge of $\overline{WR}$.
$\overline{RD}$	8	11	Reading of register data is accomplished using this pin. When CS_1 = 1, $\overline{CS_0}$ = 0 and $\overline{RD}$ = 0, the data of the register is output to $D_0 \sim D_3$. If both $\overline{RD}$ and $\overline{WR}$ are set at 0 simaltanuously, $\overline{RD}$ is to be inhibited.
$\overline{CS_0}$	2	2	Chip Select Pins. These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation. $\overline{CS_0}$ and ALE work in combination with one another, while CS_1 work independent with ALE. CS_1 must be connected to power failure detection as shown in Figure 18.
CS_1	15	20	
STD.P	1	1	Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1. Refer to Figure 9 and FUNCTIONAL DESCRIPTION OF REGISTERS.
XT	16	22	32.768 kHz crystal is to be connected to these pins. When an external clock of 32.768 kHz is to be used for MSM6242's oscillation source, either CMOS output or pull-up TTL output is to be input from XT, while $\overline{XT}$ should be left open.
$\overline{XT}$	17	23	
V_{DD}	18	24	Power supply pin. +2 ~ +6V power is to be applied to this pin.
GND	9	12	Ground pin.



The impedance of the crystal should be less than 30kΩ

Figure 8. Oscillator Circuit

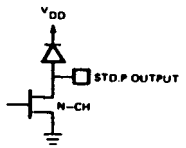


Figure 9.

FUNCTIONAL DESCRIPTION OF REGISTERS

■ $S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, M\bar{O}_1, M\bar{O}_{10}, Y_1, Y_{10}, W$

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.

b) All registers are logically positive. For example, (S8, S4, S2, S1) = 1001 which means 9 seconds.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

d) PM/AM, h_{12}, h_{10}
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the setting of 12-hour mode h_{20} is to be set. Otherwise it causes a discrepancy. In reading out the PM/AM bit in the 24-hour mode, it is continuously r[illegible] out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously r[illegible] out as 0 unless 1 is being written into this bit.

e) Registers Y1, Y10, and Leap Year. The MSM6242B is designed exclusively for the Christian Era and is capable of identifying a leap year automatically. The result of the setting of a non-existant day of the month is shown the following example: If the date February 29 or November 31, 1985, was written, it would be chang[illegible] automatically to Match 1, or December 1, 1985 at the exact time at which a carry pulse occurs for the day's digit.

f) The Register W data limits are 0–6 (Table 1 shows a possible data definition).

TABLE 1

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

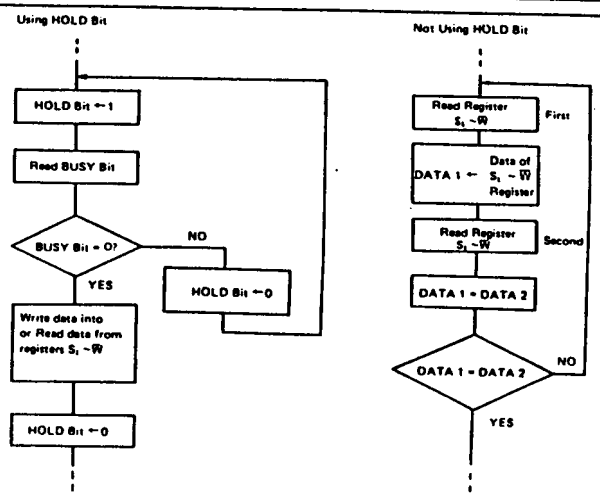
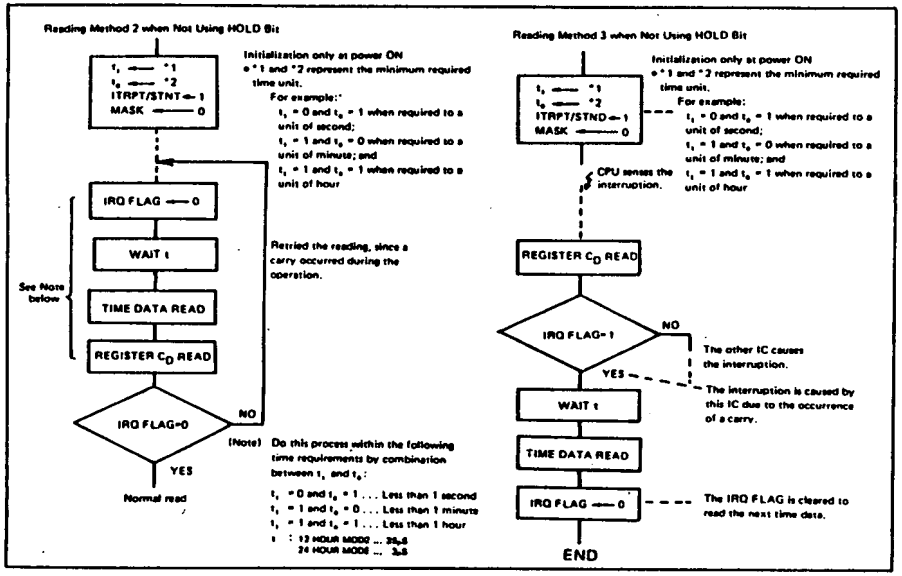


Figure 10. Reading and Writing of Registers $S_1 \sim W$



■ CD REGISTER (Control D Register)

a) HOLD (D0) – Setting this bit to a "1" inhibits the 1Hz clock to the S1 counter, at which time the Busy status bit can be read. When Busy = 0, register's $S_1 \sim \overline{W}$ can be read or written. During this procedure if a carry occurs the S1 counter will be incremented by 1 second after HOLD = 0 (this condition is guaranteed as long as HOLD = 1 does not exceed 1 second in duration). If CS1 = 0 then HOLD = 0 irrespective of any condition.

b) BUSY (D1) – Status bit which shows the interface condition with microcontroller/microprocessors. As for the method of writing into and reading from $S_1 \sim \overline{W}$ (address $\phi \sim C$), refer to the flow chart described in Figure 10.

c) IRQ FLAG (D2) – This status bit corresponds to the output level of the STD.P output. When STD.P = 0, then IRQ = 1; when STD.P =1, then IRQ = 0. The IRQ FLAG indicates that an interrupt has occurred to the microcomputer if IRQ = 1. When D0 of register CE (MASK) = 0, then the STD.P output changes according to the timing set by D3 (t_1) and D2 (t_0) of register E. When D1 of register E (ITRPT/STND) = 1 (interrupt mode), the STD.P output remains low until the IRQ FLAG is written to a "0". When IRQ = 1 and timing for a new interrupt occurs, the new interrupt is ignored. When ITRPT/STND = 0 (Standard Pulse Output mode) the STD.P output remains low until either "0" is written to the IRQ FLAG; otherwise, the IRQ FLAG automatically goes to "0" after 7.8125 ms.

When writing the HOLD or 30 second adjust bits of register D, it is necessary to write the IRQ FLAG bit to a "1".

d) ±30 ADJ (D3) – When 30-second adjustment is necessary, a "1" is written to bit D3 during which time the internal clock registers should not be read from or written to 125μs after bit D3 = 1 it will automatically return to a "0", and at that time reading or writing of registers can occur.

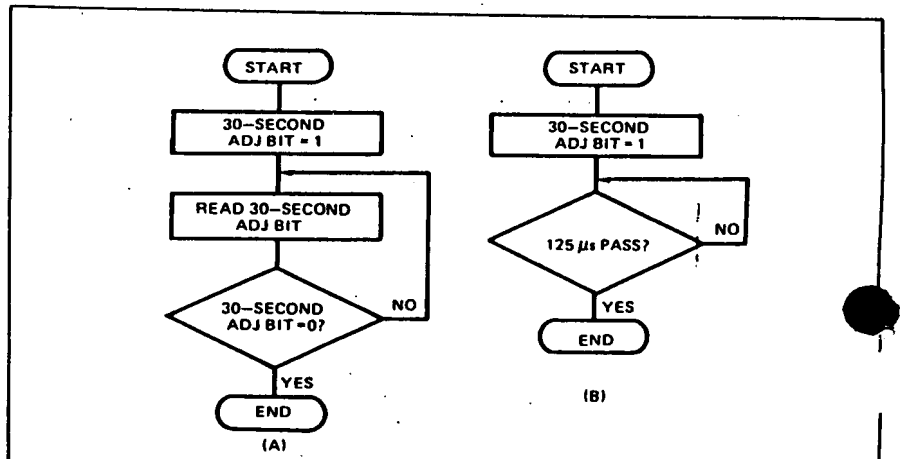


Figure 11. Writing 30-Second Adj. bit (Two Ways A, B)

■ CE REGISTER (Control E Register)

a) MASK (D0) – This bit controls the STD.P output. When MASK = 1, then STD.P = 1 (open); when MASK = 0, then STD.P = output mode. The relationship between the MASK bit and STD.P output is shown Figure 12.

b) INTRPT/STND (D1) – The INTRPT/STND input is used to switch the STD.P output between its two modes of operation, interrupt and Standard timing waveforms. When INTRPT/STND 0 a fixed cycle waveform with a low-level pulse width of 7.8125 ms is present at the STD.P output. At this time the MASK bit must equal 0, while the period in either mode is determined by T0(D2) and T1(D3) of Register E.

c) T0 (D2), T1 (D3) – These two bits determine the period of the STD.P output in both Interrupt and Fixed timing waveform modes. The tables below show the timing associated with the T0, T1 inputs as well as their relationship to INTRPT/STND and STD.P.

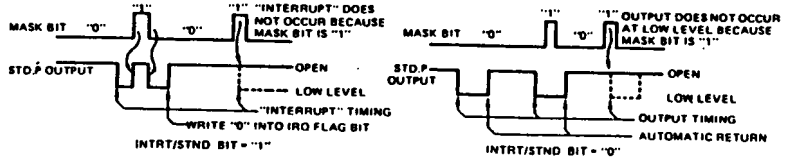
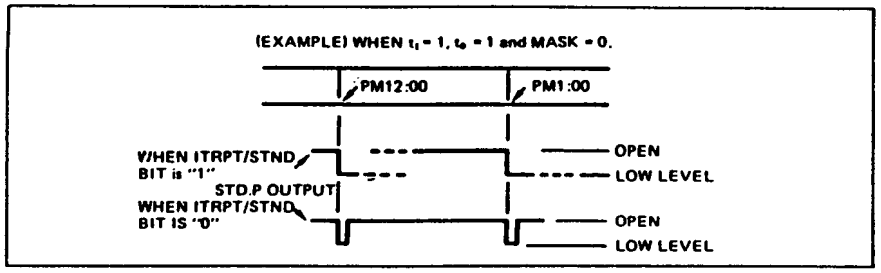


Figure 12.

t_1	t_0	Period	Duty CYCLE of "0" level when ITRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

TABLE 2

The timing of the STD.P output designated by T1 and T0 occurs the moment that a carry occurs to a clock digit.



d) The low-level pulse width of the fixed cycle waveform (ITRPT/STND = 0) is 7.8125 ms independent of T0/T1 inputs.

e) The fixed cycle waveform mode can be used for adjustment of the oscillator frequency time base. (See Figure 14).

f) During ±30 second adjustment a carry can occur that will cause the STD.P output to go low when T0/T1 = 1,0 or 1,1. However, when T1/T0 = 0, 0 and ITRPT/STND = 0, carry does not occur and the STD.P output resumes normal operation.

g) The STD.P output is held (frozen) at the point at which STOP = 1 while ITRPT/STND = 0.

h) No STD.P output change occurs as a result of writing data to registers S1 ~ H1.

■ C_F REGISTER (Control F Register)

a) REST (D0) — "RESET" — This bit is used to clear the clock's internal divider/counter of less than a second. When REST = 1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If CSI = 0 then REST = 0 automatically.

b) STOP (D1) — The STOP FLAG Only inhibits carries into the 8192Hz divider stage. There may be up to 122μs delay before timing starts or stops after changing this flag; 1 = STOP/0 = RUN.

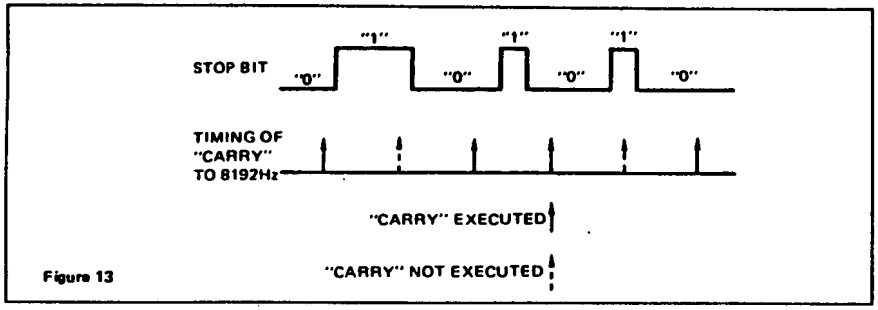


Figure 13

c) 24/12 (D2) — This bit is for selection of 24/12 hour time modes. If D2 = 1–24 hour mode is selected and the PM/AM bit is invalid. If D2 = 0–12 hour mode is selected and the PM/AM bit is valid.

"24 HOUR/ 12 HOUR" — Setting of the 24/12 hour bit is as follows:
1) REST bit = 1
2) 24/12 hour bit = 0 or 1
3) REST bit = 0
* REST bit must = 1 to write to the 24/12 hour bit.

d) TEST (d3) — When the TEST flag is a "1", the input to the SECONDS counter comes from the counter/divider stage instead of the 15th divider stage. This makes the SECONDS counter count at 5.4163KHz instead of 1Hz. When TEST = 1 (Test Mode) the STOP & REST (Reset) flags do not inhibit internal counting. When Hold = 1 during Test (Test = 1) internal counting is inhibited; however, when the HOLD FLAG goes inactive (Hold = 0) counter updating is not guaranteed.

TYPICAL APPLICATION INTERFACE WITH MSM6242B AND MICROCONTROLLERS

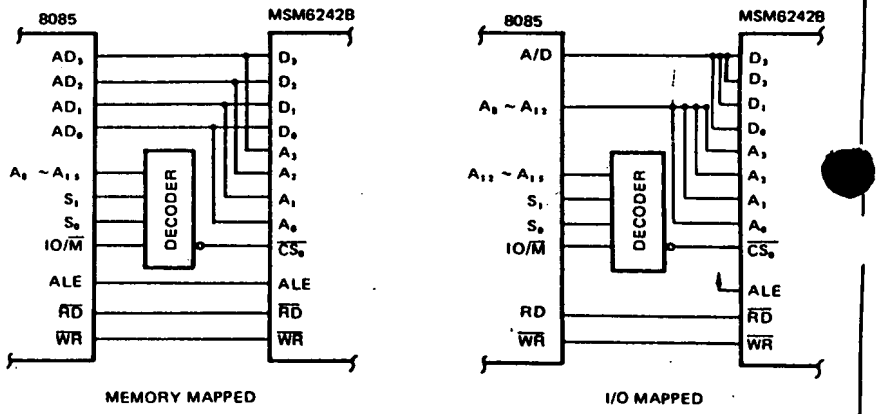


Figure 15.

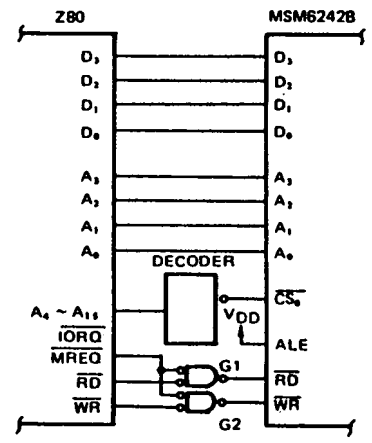


Figure 16.

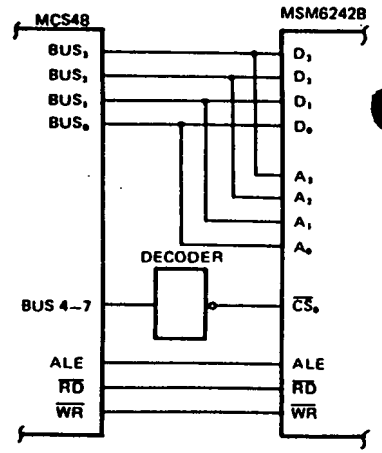


Figure 17.

TYPICAL APPLICATIONS — INTERFACE WITH MSM80C49

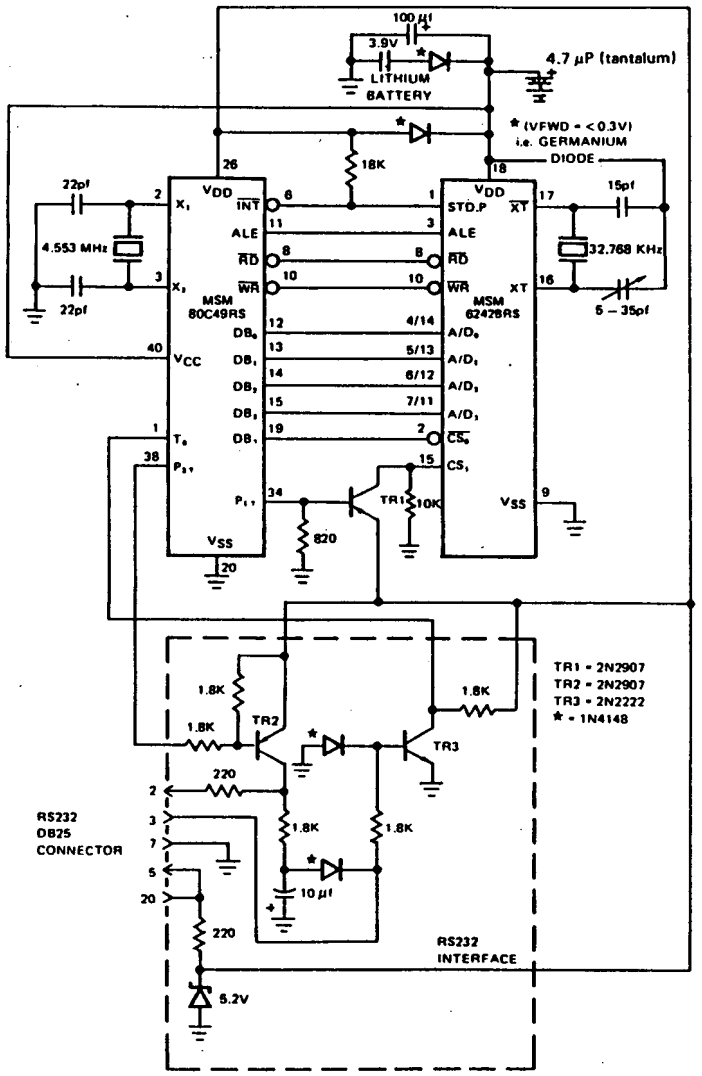
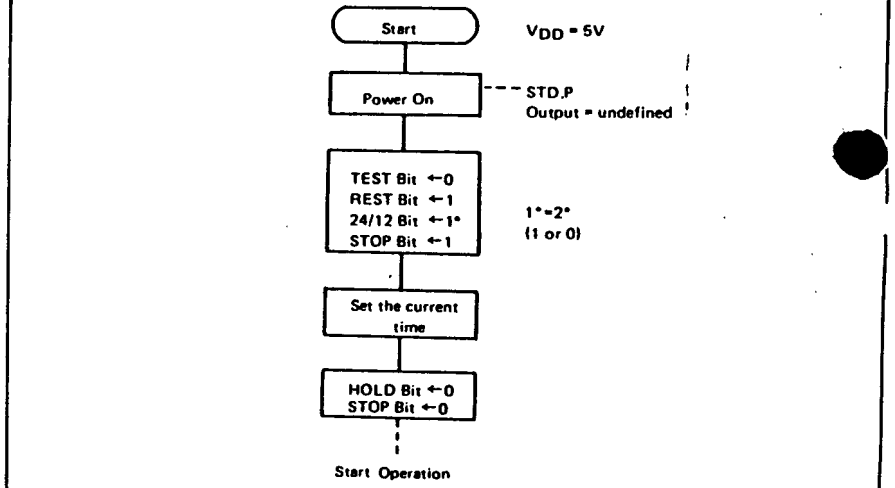


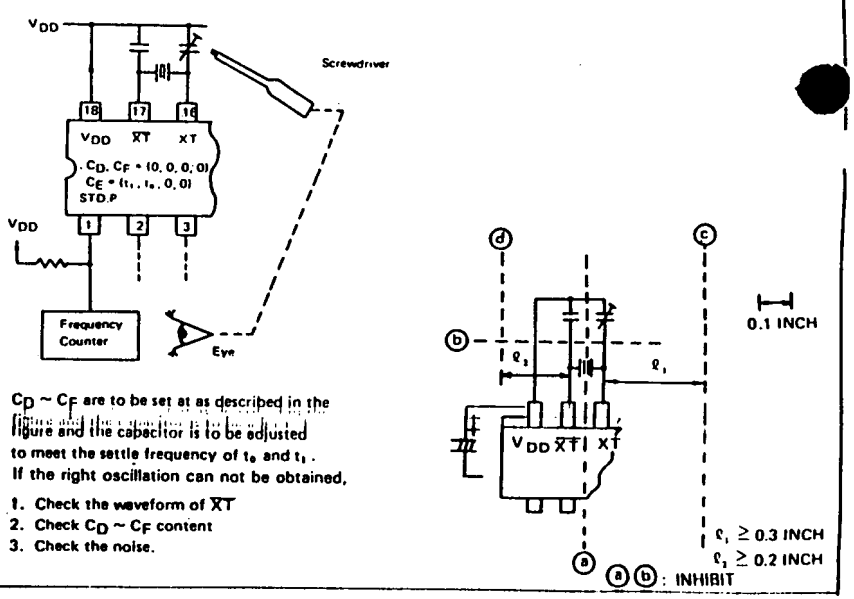
Figure 18.

APPLICATION NOTE

1. Power Supply



2. Adjustment of Frequency



C_D ~ C_F are to be set at as described in the figure and the capacitor is to be adjusted to meet the settle frequency of t_0 and t_1.
If the right oscillation can not be obtained,

1. Check the waveform of $\overline{XT}$
2. Check C_D ~ C_F content
3. Check the noise.

5

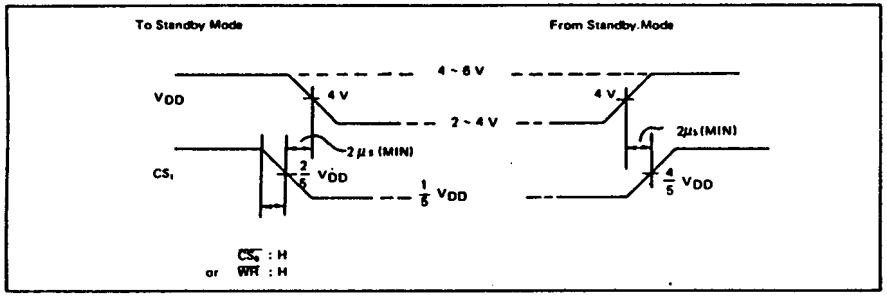
3. CH_1 (Chip Select)

V_{IH} and V_{IL} of CH_1 has 3 functions.

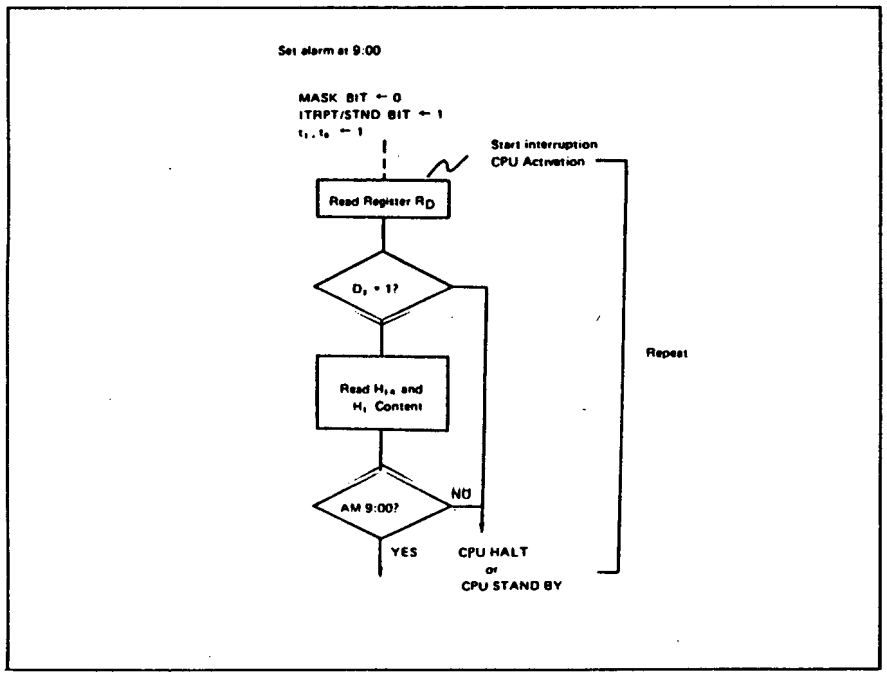
a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

a) More than 4/5 V_{DD} should be applied to the MSM6242B for the interface with a microcontroller/microprocessor in 5V operation.
b) In moving to the standby mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0V should be applied.
c) To and from the standby mode, obey following Timing chart.



4. Set STD.P at arlarm mode



TYPICAL APPLICATION – POWER SUPPLY CIRCUIT

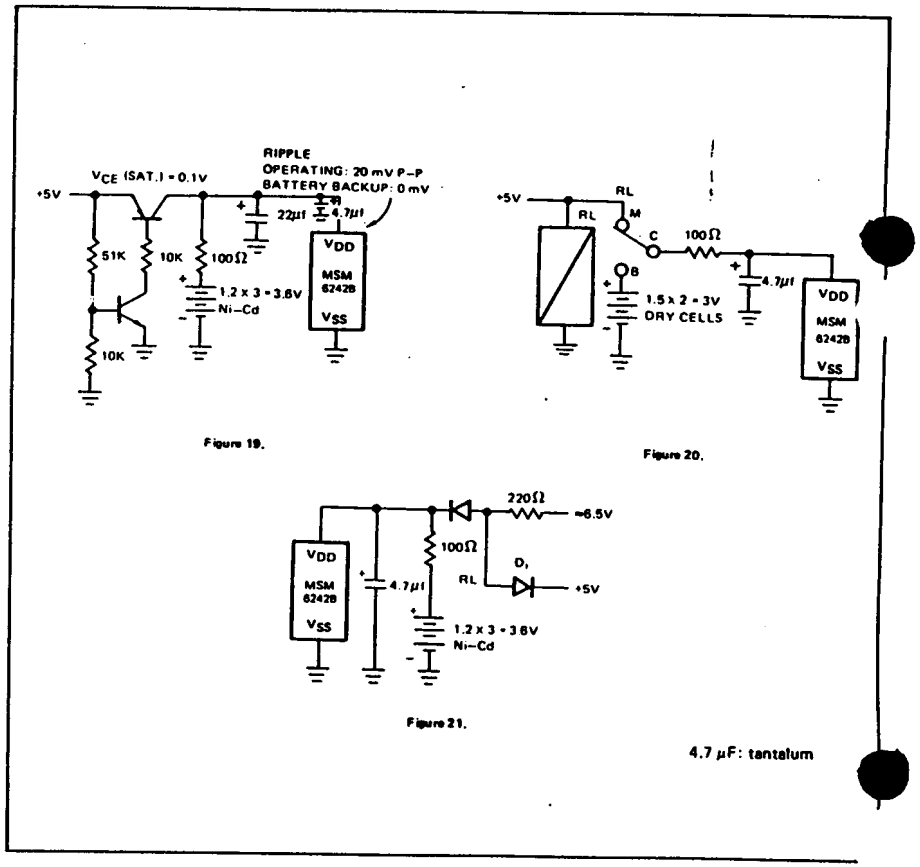


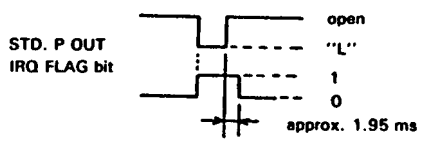
Figure 19.

Figure 20.

Figure 21.

SUPPLEMENTARY DESCRIPTION

- When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec ADJ bit and the HOLD bit, the IRQ FLAG = 1 and was generated before the writing and IRQ FLG = 1 generated in a moment then will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1"
- Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0, or ITRPT/STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.
- The relationship between SDT. P OUT and IRQ FLAG bit is shown below:



Dallas Semiconductor
Serial Timekeeper

PRELIMINARY

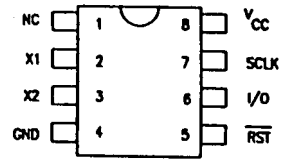
DS1202 8-Pin DIP

DS1202S 16-Pin SOIC

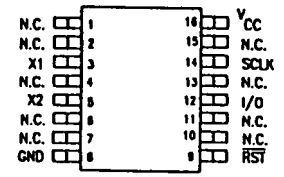
FEATURES

- Real Time clock counts seconds, minutes, hours, date of the month, day of the week and year with Leap Year compensation
- 24 x 8 RAM for scratch pad data storage
- Serial I/O for minimum pin count
- 3 volt clock operation
- Uses less than1 uA at 3 volts
- Single byte or multiple byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL compatible (V_{cc} = 5V)

PIN CONNECTIONS



8-Pin DIP



16-Pin SOIC

PIN NAMES

N.C.	-No Connection
X1, X2	-32.768 KHz Crystal Input
GND	-Ground
$\overline{RST}$	- Reset
I/O	-Data Input/Output
SCLK	-Serial Clock
V_{cc}	-Power Supply Pin

DESCRIPTION

The DS1202 contains a RealTime Clock/Calendar, 24 bytes of static RAM, and communicates with a microprocessor via a simple serial interface. The RealTime Clock/Calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for Leap Year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified using synchronous serial communication. Only three wires are required to communicate with the Clock /RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial Clock). Data can be transferred to and from the Clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 uA with voltage input, (V_{cc}) as low as three volts.

OPERATION

The main elements of the serial Timekeeper are shown in Figure 1, namely, shift register, control logic, oscillator, RealTime Clock and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Each bit is serially input on the rising edge of the clock input. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read, or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

ADDRESS/COMMAND BYTE

The address/command byte is shown in Figure 2. Each data transfer is initiated by a one byte input called the address/command byte. As defined, the MSB (Bit 7) must be a logical one. If zero, further action will be terminated. Bit 6 specifies a clock/calendar register if logic zero or a RAM location if Logical One. Bits one through five specify the designated registers to be input or output and the LSB (Bit 0) specifies a write operation (input) if logical zero or read operation output if logical one.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at location 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM Registers.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state. When data transfer is terminated to the Real-Time Clock or to RAM using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data and write cycle transfer must occur in 8-bit groups. Data transfer is illustrated in Figure 3

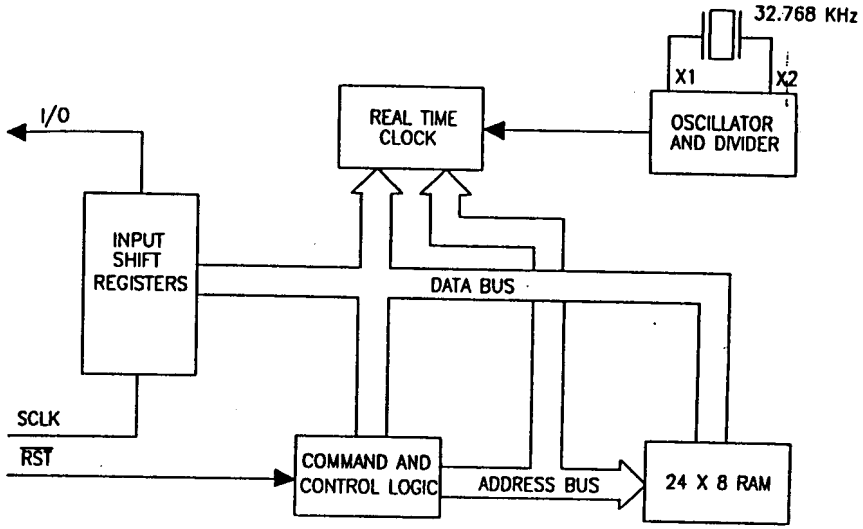
DATA INPUT

Following the eight SCLK cycles that input the write mode address/command byte (Bit 0 = Logical 0), a data byte is input on the rising edge of the next eight SCLK cycles (per byte, if burst mode is specified). Additional SCLK cycles are ignored should they inadvertently occur.

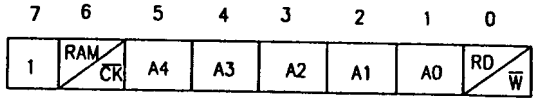
DATA OUTPUT

Following the eight SCLK cycles that input the read mode address/command byte (Bit 0 = Logical 1), a data byte is output on the falling edge of the next eight SCLK cycles (per byte, if the burst mode is specified). Note that the first data bit to be transmitted from the clock/RAM occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operaton permits continuous burst read mode capability.

DS1202 BLOCK DIAGRAM Figure 1

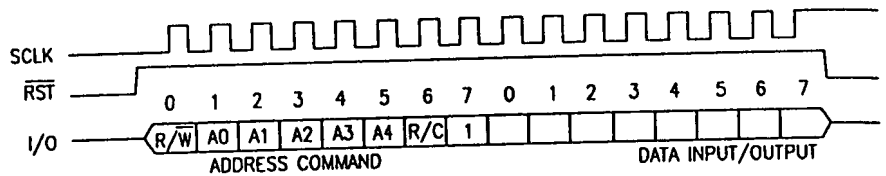


ADDRESS/COMMAND BYTE Figure 2

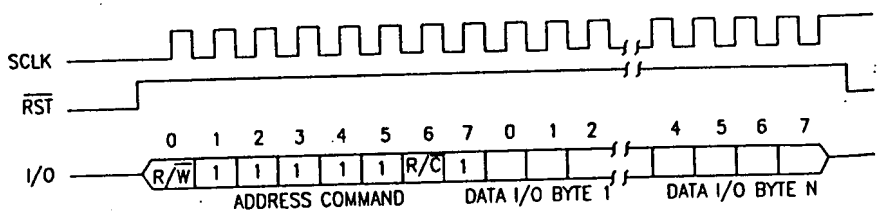


DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

518

CLOCK/CALENDAR
The Clock/Calendar is contained in eight writeable/readable registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD) except the control byte which is binary.

CLOCK HALT FLAG
Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic one, the clock oscillator is stopped and the DS1202 is placed into a low power standby mode with a current drain of less than .1 microamp. When this bit is written to logical zero, the clocks oscillator will run and keep time count from the entered value.

AM-PM/12-24 MODE
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

TEST MODE BITS
Bit 7 of the date register and bit 7 of the day register are test mode bits. These bits are forced to zero under normal operation and will always read logical zero when read.

CONTROL BYTE AND WRITE PROTECT BIT
Byte 7 of the clock/calendar registers is the write protect byte. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Bit 7 of the user byte is the write protect flag. Bit seven is set to logical one on power up and may be set high or low by writing the byte . When high, the write protect flag prevents a write operation to any internal register including both clock and RAM. Further, logic is included such that the write protect bit may be reset to a logical zero by a write operation.

CLOCK/ CALENDAR BURST MODE
Address 31 decimal of the clock/calendar address space specifies burst mode operation. In this mode the eight clock/calendar registers may be consecutively read or written. Addresses above seven (user byte) are non-existent; only addresses 0-7 are accessible.

RAM
The static RAM is contained in 24 writeable/readable registers, addressed consecutively in the RAM address space beginning at location zero.

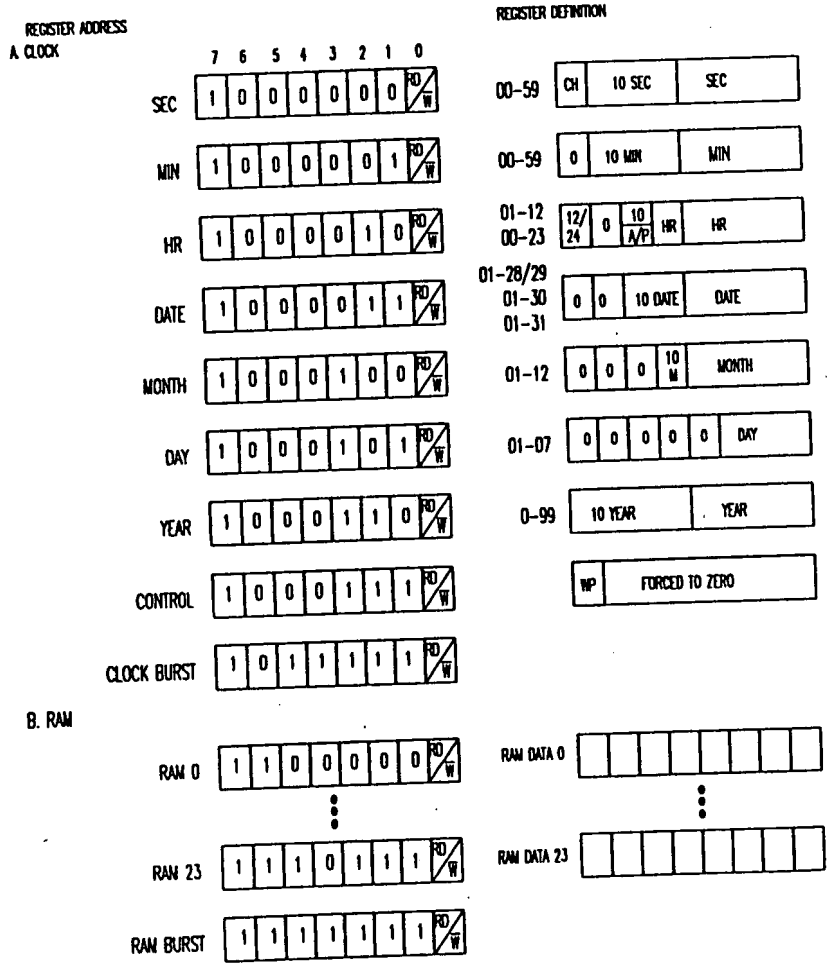
RAM BURST MODE
Addresses 31 decimal of the RAM address space specifies burst mode operation. In this mode, the 24 RAM registers may be consecutively read or written. Addresses above the maximum RAM address location are non-existent and are not accessible.

REGISTER SUMMARY
A register data format summary is shown in Figure 4.

CRYSTAL SELECTION
A 32.768 KHZ crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (x1, x2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF.

7

REGISTER ADDRESS/DEFINITION Figure 4



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND -0.5V TO +7.0V
OPERATING TEMPERATURE 0°C TO +70°C
STORAGE TEMPERATURE -55°C TO +125°C
SOLDERING TEMPERATURE -260°C FOR 10 SEC

RECOMMENDED D.C. OPERATING CONDITIONS

(0° to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply voltage	V_{CC}	4.5	5.0	5.5	VOLTS	1
Standby Supply Voltage	V_{CC1}	3.0		5.5	VOLTS	1
Logic 1 Input	V_{IH}	2.0		V_{CC}	VOLTS	1
Logic 0 Input	V_{IL}	-0.5		0.8	VOLTS	1

D.C. ELECTRICAL CHARACTERISTICS

(0° to +70°C, V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			+500	uA	6
I/O Leakage	I_{LO}			+500	uA	6
Logic 1 Output	V_{OH}	2.4			VOLTS	2
Logic 0 Output	V_{OL}			0.4	VOLTS	3
Active Supply Current	I_{CC}			4	mA	4
Standby Supply Current	I_{CC1}			1	uA	5
StandbySupply Current	I_{CC2}			100	nA	10

CAPACITANCE

(TA =25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

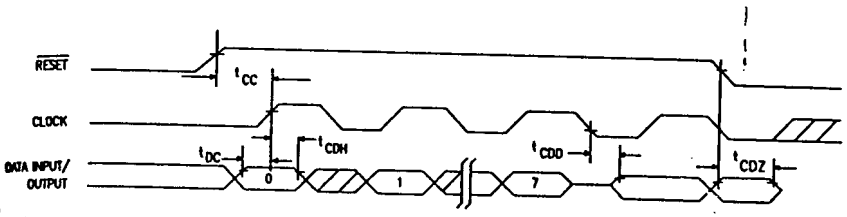
A.C. ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V ±10% 0°C TO 70°C)

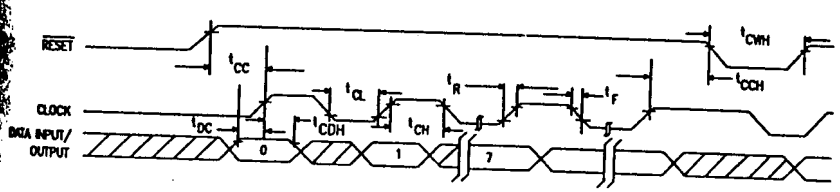
PARAMETER	SYMBOL	MIIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	7
CLK To Data Hold	t_{CDH}	70			ns	7
CLK To Data Delay	t_{CDD}			200	ns	7,8,9
CLK Low Time	t_{CC}	250			ns	7
CLK High Time	t_{CH}	250			ns	7
CLK Frequency	f_{CLK}	D.C.		2.0	MHz	7
CLK Rise &Fall	t_F			500	ns	
RST To CLK Setup	t_{CC}	1			us	7
CLK To RST Hold	t_{CCH}	60			ns	7
RST Inactive Time	t_{CWH}	1			us	7
RST To I/O High Z	t_{CDZ}			70	us	7

TIMING DIAGRAM - READ/WRITE DATA TRANSFER Figure 5

WRITE DATA TRANSFER



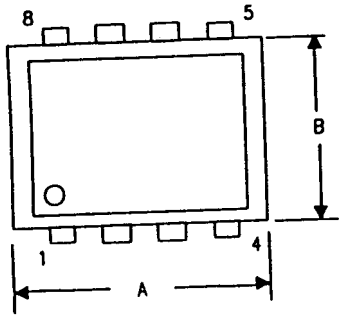
READ DATA TRANSFER



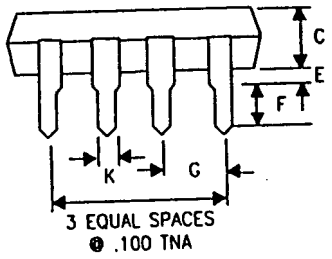
NOTES

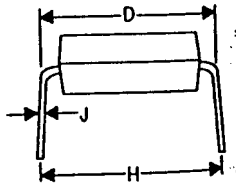
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 MA.
3. Logic zero voltages are specified at a sink current of 4 MA.
4. I_{CC} is specified with the I/O pin open.
5. I_{CC1} is specified with V_{CC} at 3.0 volts and $\overline{RST}$, I/O, and SCLK are open.
6. RST, SCLK and I/O all have 40 K ohm pull down resistors to ground.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9. Load capacitance = 50 pF.
10. I_{CC2} is specified with V_{CC} at 3.0 volts and $\overline{RST}$, I/O, and SCLK are open. The clock halt flag must also be set to logic one.

DS1202
SERIAL TIMEKEEPER
8-PIN DIP



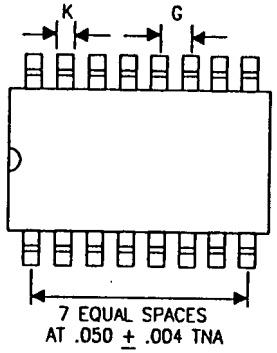
DIM.	INCHES	
	MIN.	MAX.
A	.345	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

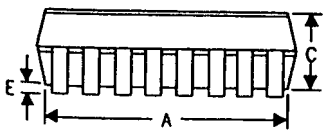


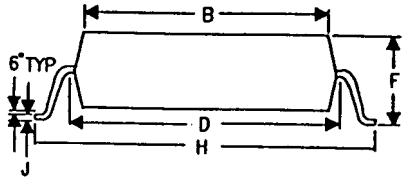


DS1202S
SERIAL TIMEKEEPER
16-PIN SOIC

DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019







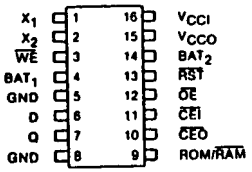
Dallas Semiconductor
TimeChip

DS1215

FEATURES

- TimeChip keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backing up RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Space saving 16-pin DIP package

PIN CONNECTIONS



PIN NAMES

Pins 1 & 2	- X_1, X_2	- 32.768 KHz Crystal Connections
Pin 3	- $\overline{WE}$	- Write Enable
Pin 4	- BAT_1	- Battery 1 Input
Pins 5 & 8	- GND	- Ground
Pin 6	- D	- Data In
Pin 7	- Q	- Data Out
Pin 9	- ROM/$\overline{RAM}$	- ROM-RAM Select
Pin 10	- $\overline{CEO}$	- Chip Enable Out
Pin 11	- $\overline{CEI}$	- Chip Enable Input
Pin 12	- $\overline{OE}$	- Output Enable
Pin 13	- $\overline{RST}$	- Reset
Pin 14	- BAT_2	- Battery 2 Input
Pin 15	- V_{CCO}	- Switched Supply Output
Pin 16	- V_{CCI}	- +5V DC Input

NOTE: Both pins 5 and 8 must be grounded.

DESCRIPTION

The DS1215 is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch provides hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last date of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator, or a 24-hour mode.

The nonvolatile memory controller portion of the circuit is designed to handle power fail detection, memory write protection, and battery redundancy. In short, the controller changes standard CMOS memories into nonvolatile memories, and provides continuous power to the TimeChip. Alternatively the TimeChip can be used with ROM memory by controlling the Chip Enable Output signal ($\overline{CEO}$) while the TimeChip is being accessed.

OPERATION

The block diagram of Figure 3 illustrates the main elements of the TimeChip. Communication with the TimeChip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on Data In (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the Chip Enable Output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the TimeChip and Chip Enable Output remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the TimeChip starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the TimeChip. These 64 write cycles are used only to gain access to the TimeChip.

When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is *not* found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 1). With a correct match for 64 bits, the TimeChip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the TimeChip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the TimeChip.

A 32,768 Hz quartz crystal, Daiwa part no. DT-26S or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X_1, X_2). The crystal selected for use should have a specified load capacitance of 6 pF.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the TimeChip is determined by the level of the ROM/$\overline{RAM}$ select pin. When ROM/$\overline{RAM}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. First a switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.2 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS static RAM. The DS1215 also performs redundant battery control for high reliability. On power fail the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground. The DS1215 provides the function of safeguarding the TimeChip and RAM data by power fail detection and write protection. Power fail detection occurs when V_{CCI} falls below VTP which is equal to $1.26 \times V_{BAT}$. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power fail signal to the control logic. The power fail signal forces the chip enable output ($\overline{CEO}$) to V_{CCI} or $V_{BAT} - 0.2$ volts for external RAM write protection. During nominal supply conditions, $\overline{CEO}$ will track $\overline{CEI}$ with a maximum propagation delay of 20 ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the TimeChip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/TimeChip interface is illustrated in Figure 4.

When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device which retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force $\overline{CEO}$ high when power fails. However, the TimeChip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/TimeChip interface is illustrated in Figure 5.

TIMECHIP COMPARISON REGISTER DEFINITION Figure 1

	7	6	5	4	3	2	1	0	
Byte 0	1	1	0	0	0	1	0	1	C5
Byte 1	0	0	1	1	1	0	1	0	3A
Byte 2	1	0	1	0	0	0	1	1	A3
Byte 3	0	1	0	1	1	1	0	0	5C
Byte 4	1	1	0	0	0	1	0	1	C5
Byte 5	0	0	1	1	1	0	1	0	3A
Byte 6	1	0	1	0	0	0	1	1	A3
Byte 7	0	1	0	1	1	1	0	0	5C

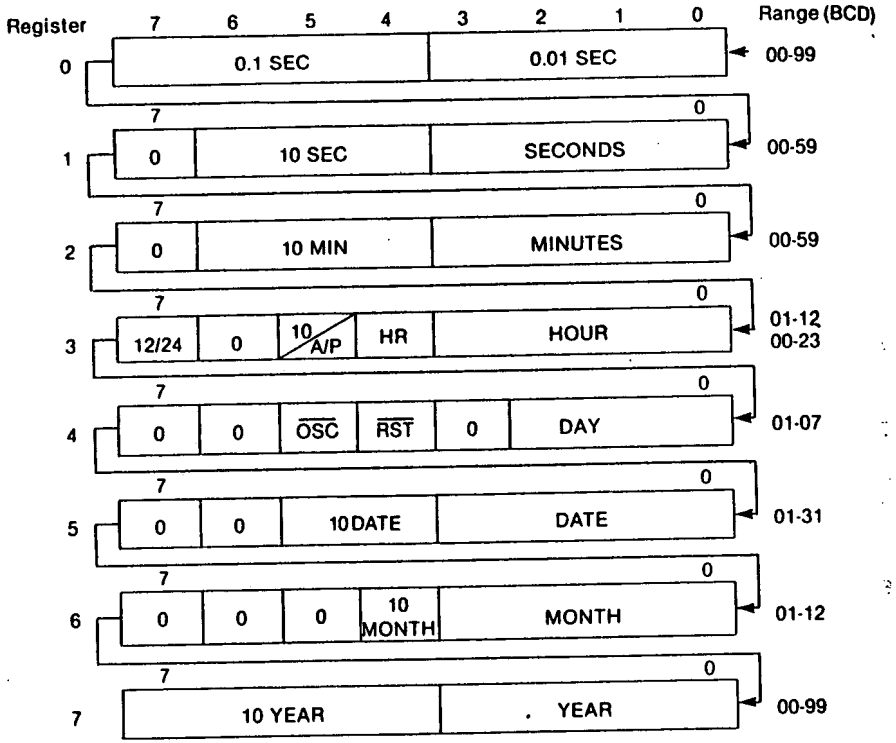
Note:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the TimeChip is less than 1 in 10^{19}.

TIMECHIP REGISTER INFORMATION

The TimeChip information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the TimeChip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the TimeChip registers are not binary coded decimal format (BCD) in 12-hour mode. Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

TIMECHIP REGISTER DEFINITION Figure 2

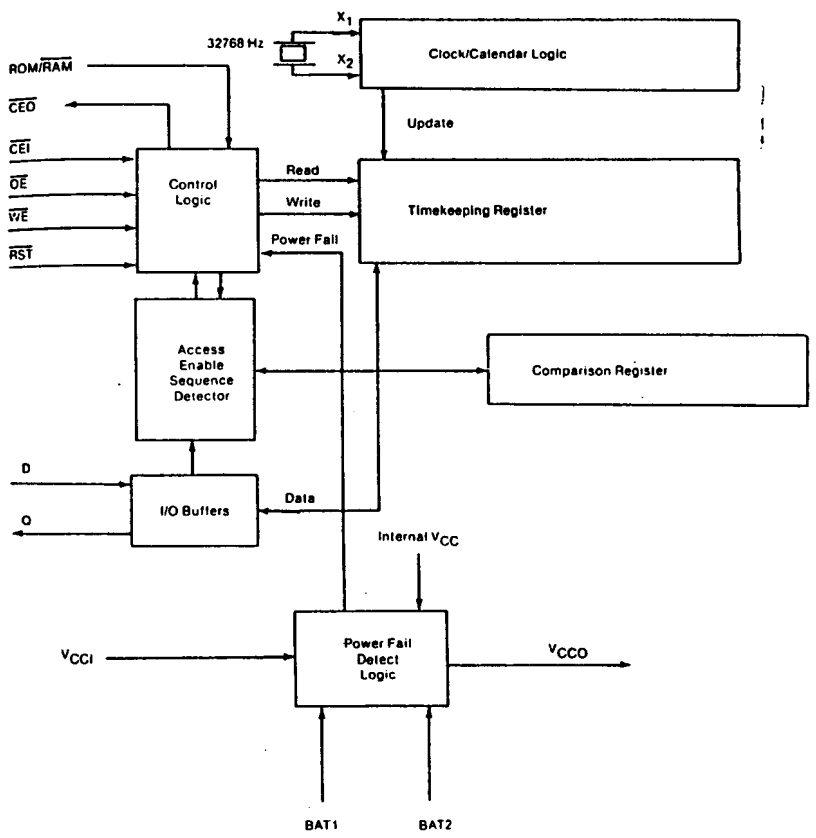


AM-PM/12/24 MODE
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

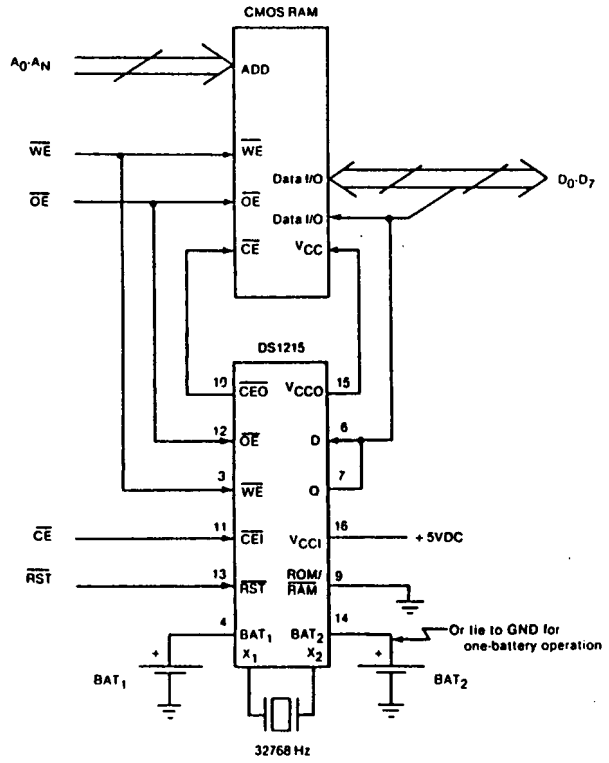
OSCILLATOR AND RESET BITS
Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the TimeChip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to Logic 0 the oscillator turns on and the watch becomes operational.

ZERO BITS
Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

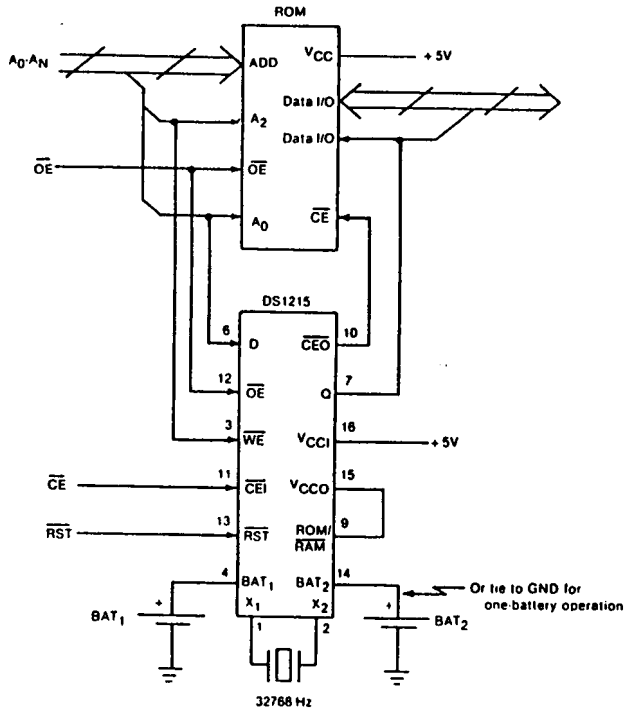
TIMECHIP BLOCK DIAGRAM Figure 3



RAM/TIMECHIP INTERFACE Figure 4



ROM/TIMECHIP INTERFACE Figure 5



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO} = V_{CCI} - 0.2$	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	−1.0		+1.0	μA	
Output Leakage	I_{LO}	−1.0		+1.0	μA	
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C, V_{CC} < 4.5V)

$\overline{CEO}$ Output	V_{OH1}	V_{CCI} or $V_{BAT}-0.2$			V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			1	μA	6
Battery Backup Current @$V_{CCO} = V_{BAT} - 0.2V$	I_{CCO2}			10	μA	10

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

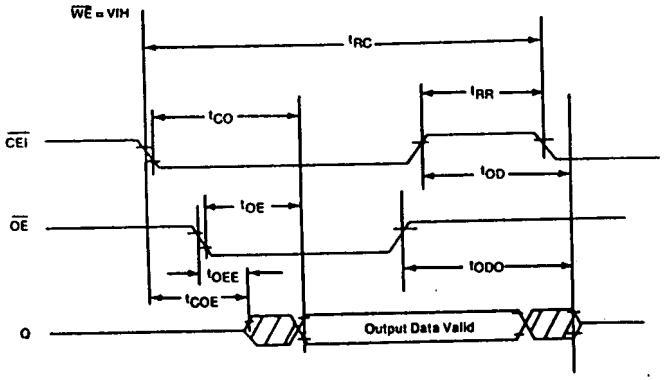
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = GND (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$I Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$I To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$I To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{CE}$I Pulse Width	t_{CW}	170			ns	
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$I Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{CE}$I High to Power Fail	t_{PF}			0	ns	

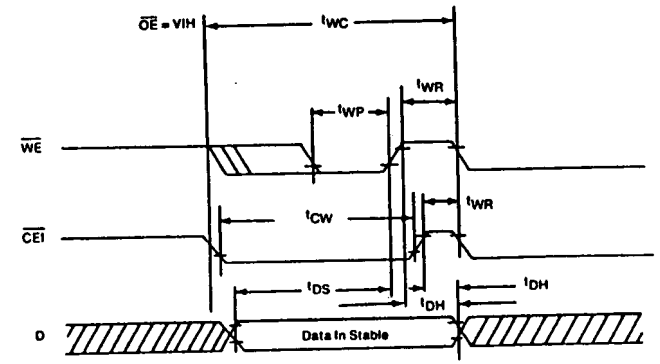
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

TIMING DIAGRAM—READ CYCLE TO TIMECHIP ROM/$\overline{\text{RAM}}$ = GND



TIMING DIAGRAM—WRITE CYCLE TO TIMECHIP ROM/$\overline{\text{RAM}}$ = GND



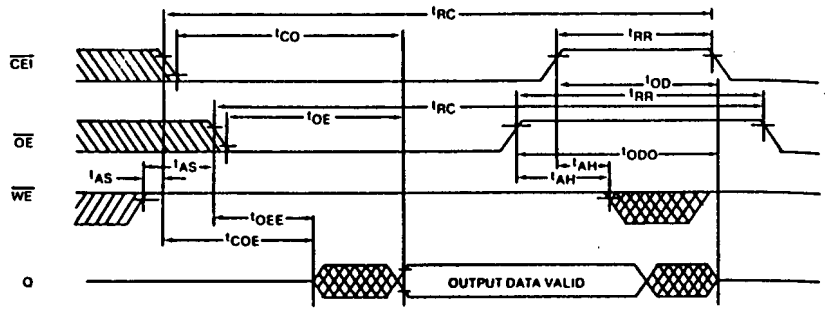
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{\text{RAM}}$ = V_{CCO} (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{\text{CEI}}$ Access Time	t_{CO}			200	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			200	ns	1
$\overline{\text{CEI}}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{\text{OE}}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{\text{CEI}}$ to Output in High Z	t_{OD}			100	ns	
$\overline{\text{OE}}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{\text{CEI}}$ Pulse Width	t_{CW}	170			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up Time	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{\text{RST}}$ Pulse Width	t_{RST}	200			ns	
$\overline{\text{CEI}}$ Propagation Delay	t_{PD}	5	10	20	ns	2,3
$\overline{\text{CEI}}$ High to Power Fail	t_{PF}			0	ns	

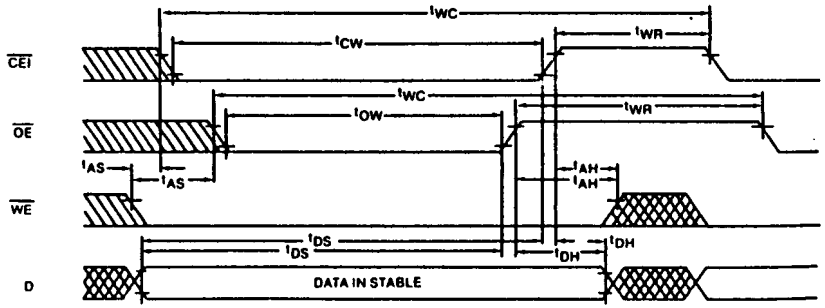
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

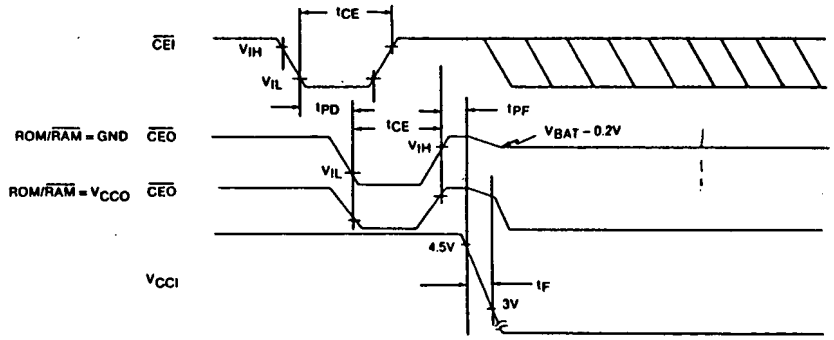
TIMING DIAGRAM—READ CYCLE ROM/$\overline{RAM}$ = V_{CCO}



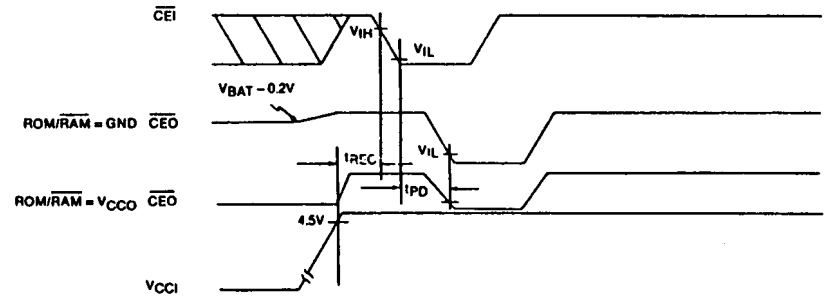
TIMING DIAGRAM—WRITE CYCLE ROM/$\overline{RAM}$ = V_{CCO}



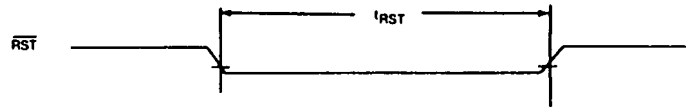
TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



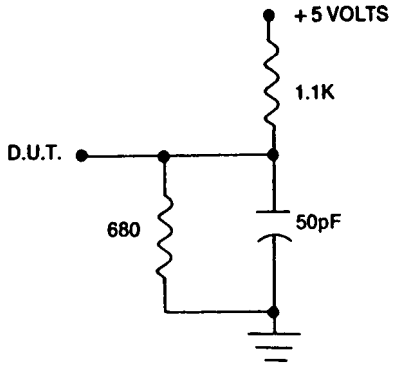
TIMING DIAGRAM—RESET FOR TIMECHIP



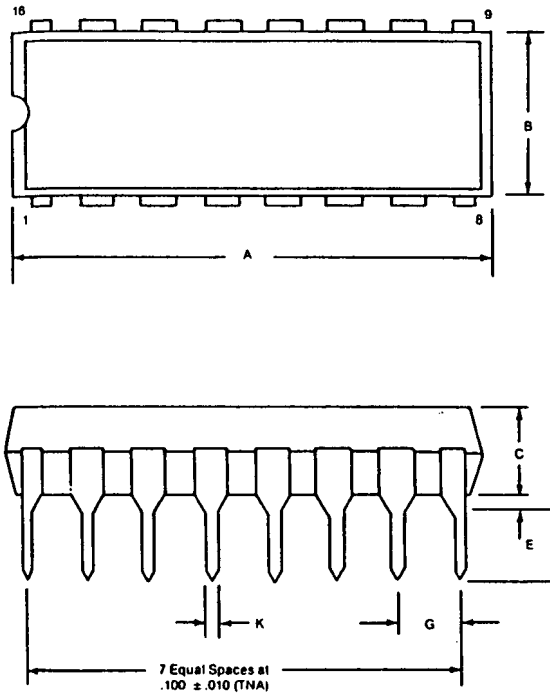
NOTES

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10 ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power fail detect. $V_{TP} = 1.26 \times V_{BAT}$ For 10% operation $V_{BAT} = 3.5V$ max.; for 5% operation $V_{BAT} = 3.7V$ max.
8. I_{CCO1} is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CCO2} is the maximum average load current which the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

OUTPUT LOAD Figure 6



DS1215 TimeChip 16-Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

Dallas Semiconductor
WATCHDOG TIMEKEEPER

PRELIMINARY
DS1286

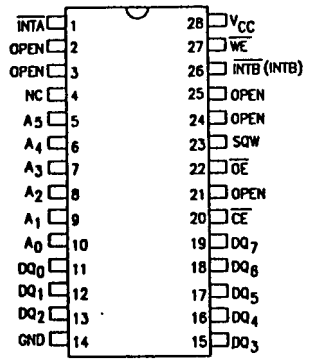
FEATURES

- Watchdog Timekeeper keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months and years
- Watchdog Timer restarts an out of control processor
- Alarm function schedules real time related activities
- Embedded lithium energy cell maintains time, Watchdog, user RAM and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than 1 minute/month at 25° C
- Greater than 10 years of timekeeping in the absence of Vcc
- 50 bytes of user NV RAM

DESCRIPTION

The DS1286 Watchdog Timekeeper is a self contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates need for any external circuitry. Data contained within 64 eight bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of Vcc and write protects memory when Vcc is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of Vcc. The Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The Watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

PIN DESCRIPTION



PIN NAMES

$\overline{INTA}$	- Interrupt Output A
$\overline{INTB}$(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
$\overline{CE}$	- Chip Enable
$\overline{OE}$	- Output Enable
$\overline{WE}$	- Write Enable
Vcc	- +5 Volts
GND	- Ground
N.C.	- No Connection
OPEN	- Pin Missing
SQW	- Square Wave Output

OPERATION - READ REGISTERS

The DS1286 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ and $\overline{OE}$ are active (LOW). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1286 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

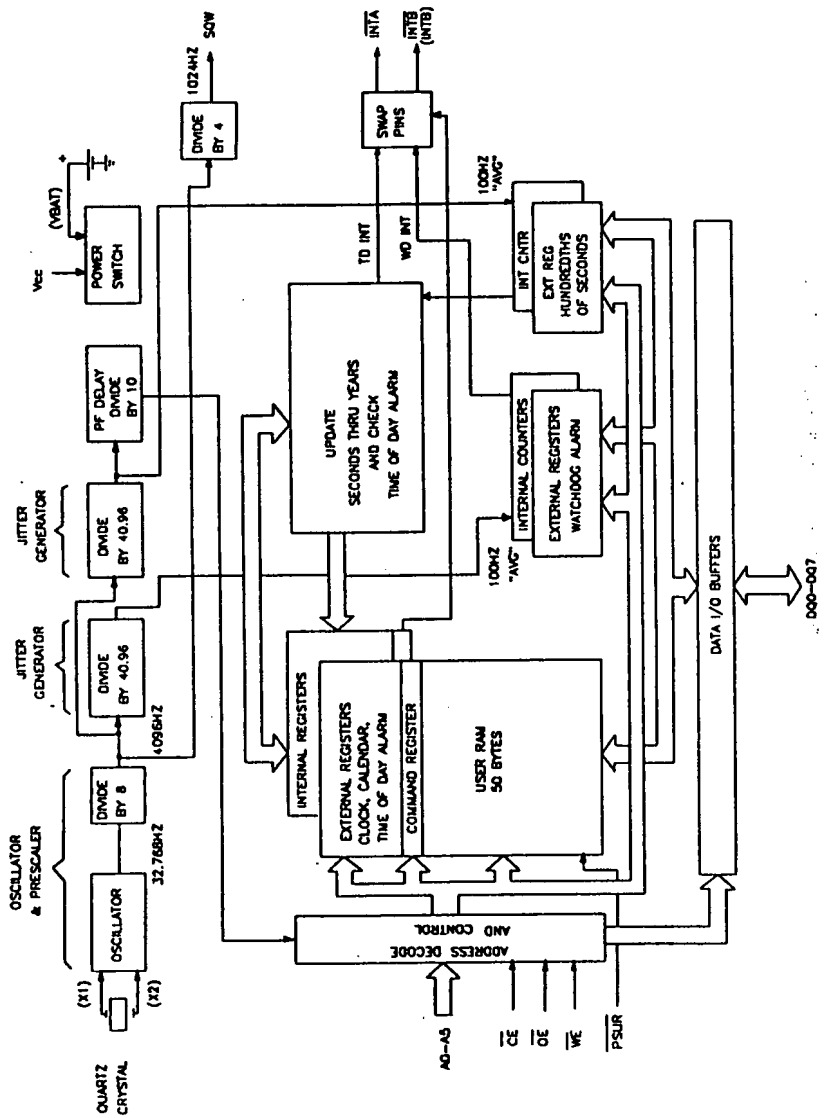
DATA RETENTION

The Watchdog Timekeeper provides full functional capability when Vcc is greater than 4.5 volts and write protects the register contents at 4.25 volts typical. Data is maintained in the absence of Vcc without any additional support circuitry. The DS1286 constantly monitors Vcc. Should the supply voltage decay, the Watchdog TimeKeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of Vcc. As Vcc falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc and disconnects the internal lithium energy source. Normal operation can resume after Vcc exceeds 4.5 volts for a period of 150 ms.

WATCHDOG TIMEKEEPER REGISTERS

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm and Watchdog Registers are memory locations which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9 and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Register C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register E through Register 3F are user bytes and can be used to contain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9 and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logical zero, $\overline{EOSC}$ (Bit 7) enables the Real Time Clock oscillator. This bit is set to logical one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 24). When set to logical zero, the Square Wave Output Pin will output a 1024 HZ Square Wave Signal. When set to logic one the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic one, the 12 Hour Format is selected. In the 12 Hour Format, Bit 5 is the AM/PM Bit with logical one being PM. In the 24 Hour Mode, Bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (Bit 7 of Register B) is set low or the clock oscillator is not running.

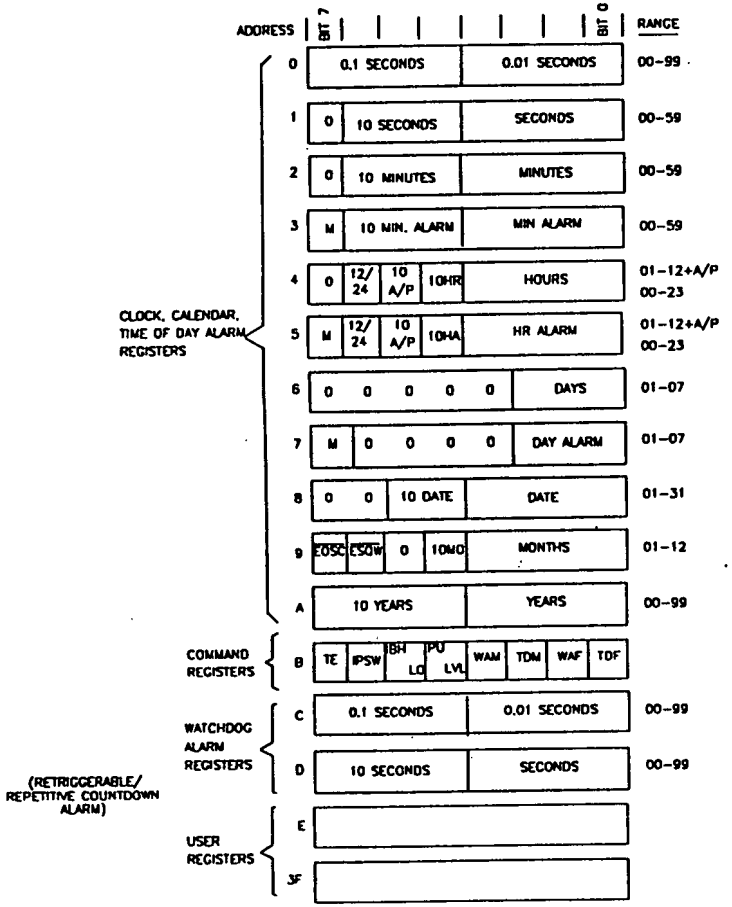
The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day Registers at the present recorded time allowing access to occur without danger of simultaneous update. When the watch registers have been read or written a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers are continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logical zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when Bit 7 of Register 7 is set to a logical one. Similarly, an alarm is generated every hour when Bit 7 of Registers 7 and 5 is set to a logical 1. When Bit 7 of Registers 7, 5, and 3 is set to a logical 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logical one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm Registers. However, if the transfer enable bit is set to logical zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logical one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logical one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logical zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask Bit (WAM). When this bit is written to a logical one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm Registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. Output $\overline{\text{INTB}}$ (INTB) will either sink or source current for a minimum of 3 ms depending on the level of Bit 5. When Bit 5 is set to logic one, the B Interrupt will source current. When Bit 5 is set to logical zero, the B Interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ (INTB). When set to logical one, $\overline{\text{INTA}}$ becomes the Time of Day Alarm Interrupt Pin and $\overline{\text{INTB}}$ (INTB) becomes the Watchdog Interrupt Pin. When Bit 6 is set to logical zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on $\overline{\text{INTB}}$ (INTB) and the Watchdog Interrupt will be output on $\overline{\text{INTA}}$. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day Registers.

ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND -0.3V TO +7.0V
OPERATING TEMPERATURE 0°C TO 70°C
STORAGE TEMPERATURE -40°C TO +70°C
SOLDERING TEMPERATURE 260°C FOR 10 SEC.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{cc}	4.5	5.0	5.5	V	10
INPUT LOGIC 1	V_{IH}	2.2		V_{cc} + 0.3	V	10
INPUT LOGIC 0	V_{IL}	-0.3		+0.8	V	10

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc =5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT	I_{IL}	-1.0		+1.0	uA	
OUTPUT LEAKAGE CURRENT	I_{LO}	-1.0		+1.0	uA	
I/O LEAKAGE CURRENT	I_{LIO}	-1.0		+1.0	uA	
OUTPUT CURRENT @ 2.4V	I_{OH}	-1.0			mA	
OUTPUT CURRENT @ 0.4V	I_{OL}	2.0			mA	13
STANDBY CURRENT $\overline{CE}$= 2.2V	I_{CCS1}		3.0	7.0	mA	
STANDBY CURRENT $\overline{CE}$ ≥ Vcc -0.5	I_{CCS2}			4.0	mA	
ACTIVE CURRENT	I_{CC}			15	mA	
WRITE PROTECTION VOLTAGE	V_{TP}		4.25		V	

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CAPACITANCE

(T_A=25°C)

PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
INPUT CAPACITANCE	C_{IN}	7	10	pF	
OUTPUT CAPACITANCE	C_{OUT}	7	10	pF	
INPUT/OUTPUT CAPACITANCE	C_{IO}	7	10	pF	

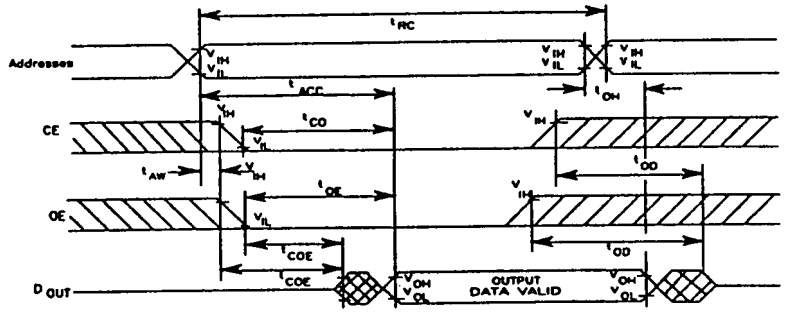
A.C. ELECTRICAL CHARACTERISTICS

(0° C to 70° C, Vcc =4.5v to 5.5v)

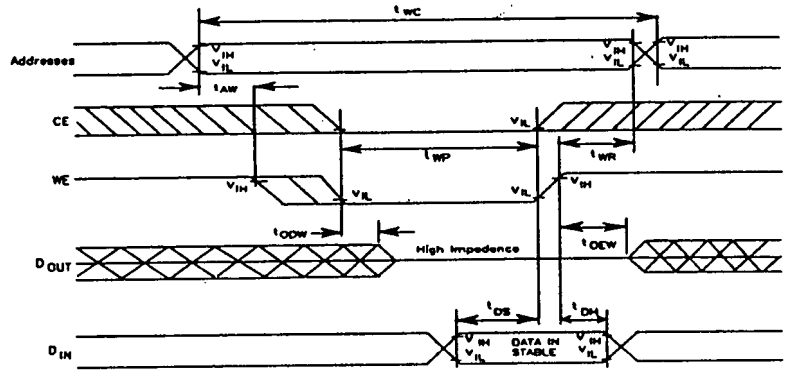
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
READ CYCLE TIME	t_{RC}	150			ns	1
ADDRESS ACCESS TIME	t_{ACC}			150	ns	
$\overline{CE}$ ACCESS TIME	t_{CO}			150	ns	
$\overline{OE}$ ACCESS TIME	t_{OE}			75	ns	
$\overline{OE}$ OR $\overline{CE}$ TO OUTPUT ACTIVE	t_{COE}	10			ns	
OUTPUT HIGH Z FROM DESELECT	t_{OD}			75	ns	
OUTPUT HOLD FROM ADDRESS CHANGE	t_{OH}	10			ns	
WRITE CYCLE TIME	t_{WC}	150			ns	
WRITE PULSE WIDTH	t_{WP}	140			ns	3
ADDRESS SETUP TIME	t_{AW}	0			ns	
WRITE RECOVERY TIME	t_{WR}	10			ns	
OUTPUT HIGH Z FROM $\overline{WE}$	t_{ODW}			50	ns	
OUTPUT ACTIVE FROM $\overline{WE}$	t_{OEW}	10			ns	
DATA SETUP TIME	t_{DS}	60			ns	4
DATA HOLD TIME	t_{DH}	0			ns	4,5
$\overline{INTA}$, $\overline{INTB}$ PULSE WIDTH	t_{IPW}	3			ms	11,12

7

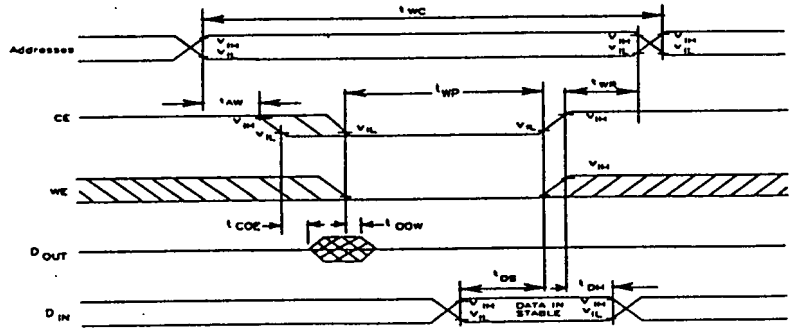
READ CYCLE (1)



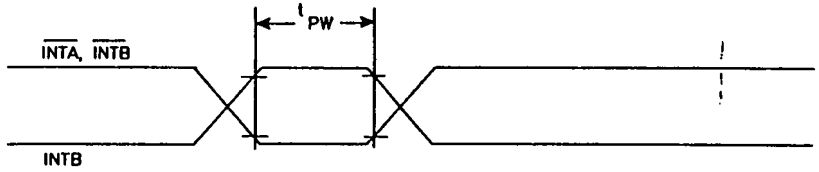
WRITE CYCLE 1 (2), (6), (7)



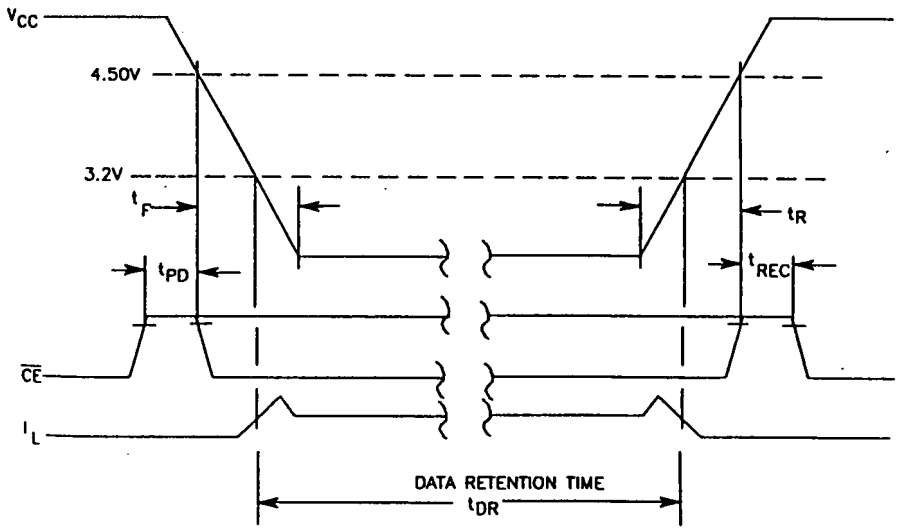
WRITE CYCLE 2 (2), (8)



TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



LEAKAGE CURRENT I_L SUPPLIED FROM LITHIUM CELL

POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at VIH before Power Down	0		us	
t_F	VCC slew from 4.5V to 0V ($\overline{CE}$ at VIH)	350		us	
t_R	VCC slew from 0V to 4.5V ($\overline{CE}$ at VIH	100		us	
t_{REC}	$\overline{CE}$ at VIH after Power Up		150	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES
1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the Output Buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "and" of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt Output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$ (INTB) are open drain outputs.

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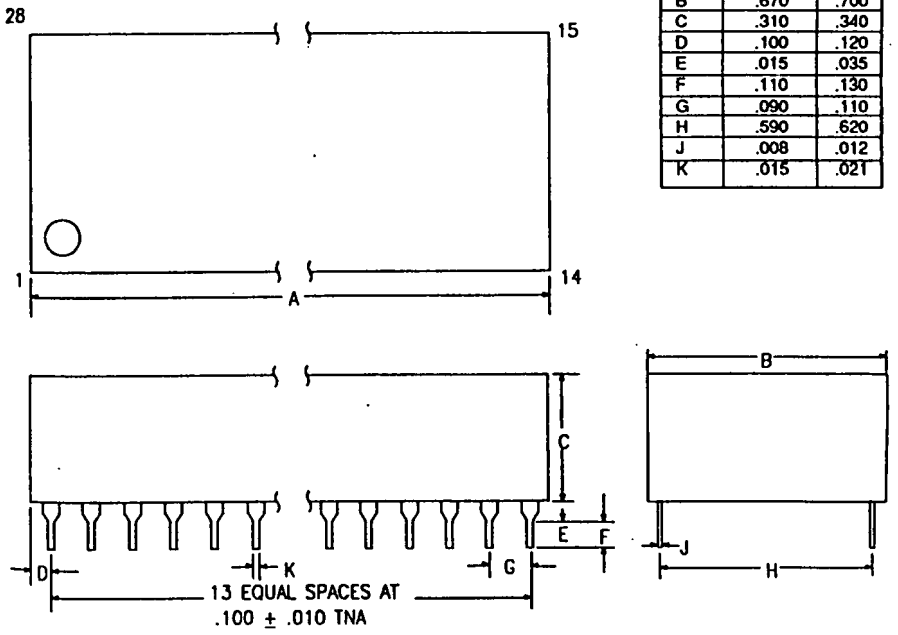
A.C. TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1286
WATCHDOG TIMEKEEPER

DIM.	INCHES	
	MIN	MAX
A	1.520	1.540
B	.670	.700
C	.310	.340
D	.100	.120
E	.015	.035
F	.110	.130
G	.090	.110
H	.590	.620
J	.008	.012
K	.015	.021



7

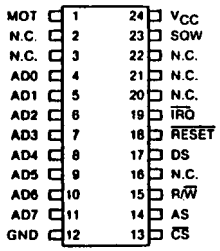
Dallas Semiconductor
Real Time Clock

DS1287

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 *us* to 500 ms
  - End of clock update cycle

PIN CONNECTIONS



PIN NAMES

AD0 - AD7	-	Multiplexed Address/Data Bus
N.C.	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground

DESCRIPTION

The DS1287 RealTime Clock Plus RAM is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The RealTime Clock Plus RAM is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connection with the major internal functions of the DS1287 Real Time Clock Plus RAM. The following paragraphs describe the function of each pin.

POWER DOWN/POWER UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin and DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal Lithium energy source supplies power to the Real Time Clock and the RAM memory.

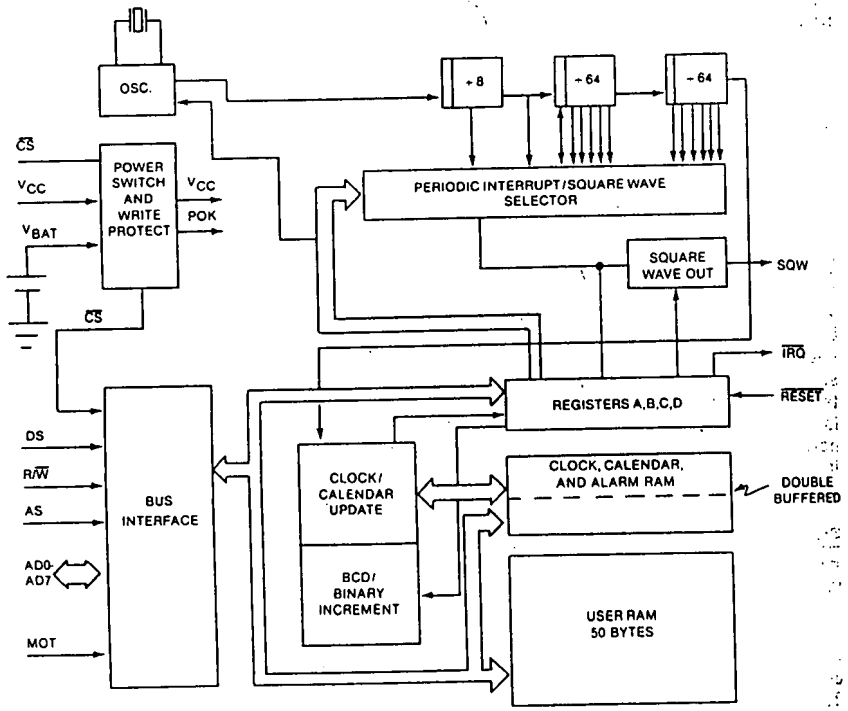
SIGNAL DESCRIPTIONS

GND, V_{CC}—D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and TimeKeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select)—The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

SQW (Square Wave Output)—The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

BLOCK DIAGRAM DS1287 Figure 1



PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				tpI PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 *us*	8.192 KHz
0	1	0	0	244.141 *us*	4.096 KHz
0	1	0	1	488.281 *us*	2.048 KHz
0	1	1	0	976.5625 *us*	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus)—Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input)—A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

DS (Data Strobe or Read Input)—The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read ($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS1287 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input)—The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input)—The Chip Select signal ($\overline{CS}$) must be asserted low for a bus cycle in which the DS1287 is to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output)—The $\overline{IRQ}$ pin is an active low output of the DS1287 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pullup resistor.

RESET (Reset Input)—The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer which controls the DS1287 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{RESET}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{IRQ}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{SQWE}$) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{RESET}$ may be connected to V_{CC}. This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

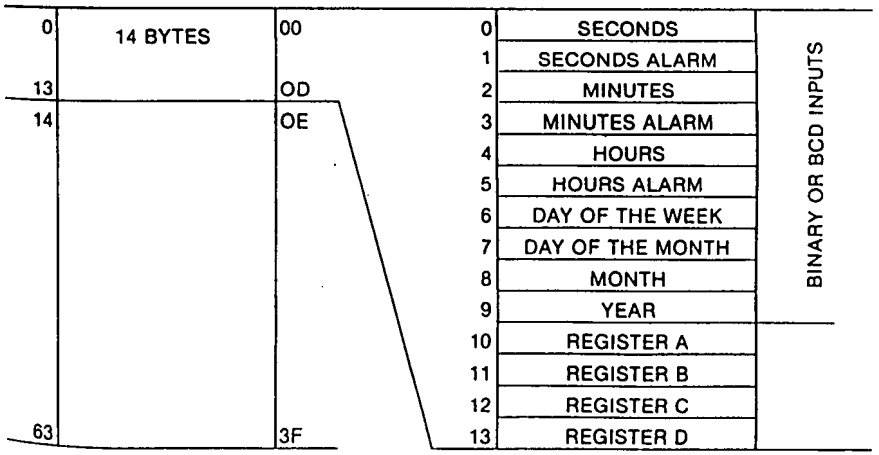
ADDRESS MAP

The Address Map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A, B, C, and D) are described in the "Register" section.

ADDRESS MAP DS1287 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logical one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

TIME CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours - 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours - 24-hr Mode	0-23	00-17	00-23
5	Hours Alarm - 12-hr	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm - 24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any

hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 500 ms to 122 μs. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS
When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the Lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION
Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION
The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 *us*. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs,create output intervals, or await the next needed software function.

UPDATE CYCLE
The DS1287 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

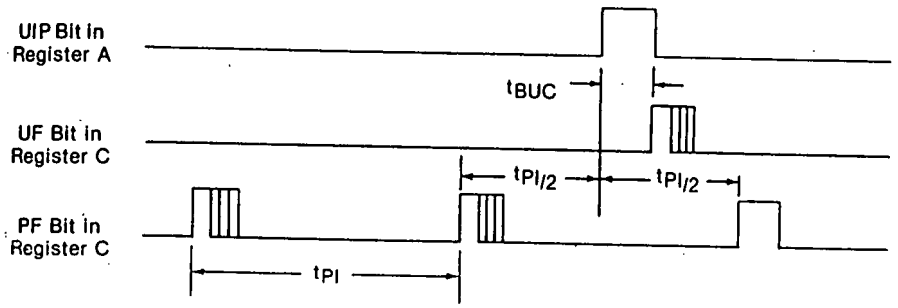
There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 *us* later. If a low is read on the UIP bit, the user has at least

244 *us* before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 *us*.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI}/2+t_{BUC}$) to insure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.

t_{BUC} = Delay time before update cycle = 244 *us*.

REGISTERS
The DS1287 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP
The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2
These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0
These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET
When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the DS1287.

PIE
The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE
The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

UIE
The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE
When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM
The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12
The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

DSE
The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF
The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

i.e., IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF
The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF
A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF
The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3
These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT
The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal Lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0
The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*
Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
I/O Leakage	I_{LO}	-1.0		+1.0	uA	4
Input Current	I_{MOT}	-1.0		+500	uA	3
Output @2.4V	I_{OH}	-1.0			mA	1,5
Output @0.4V	I_{OL}			4.0	mA	1

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

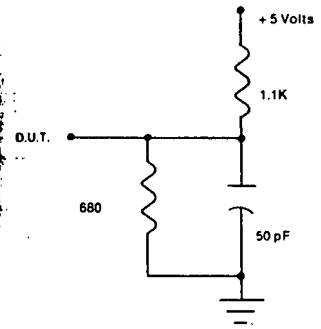
(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		D.C.	ns	
Pulse Width, DS/E Low or RD/WR High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/WR Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/W Hold Time	t_{RWH}	10			ns	
R/W Set-Up Time Before DS/E	t_{RWS}	50			ns	
Chip Select Set-Up Time Before DS, WR or RD	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or RD	t_{DDR}	20		120	ns	6
Data Set-Up Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			us	
IRQ Release from DS	t_{IRDS}			2	us	
IRQ Release from RESET				2	us	

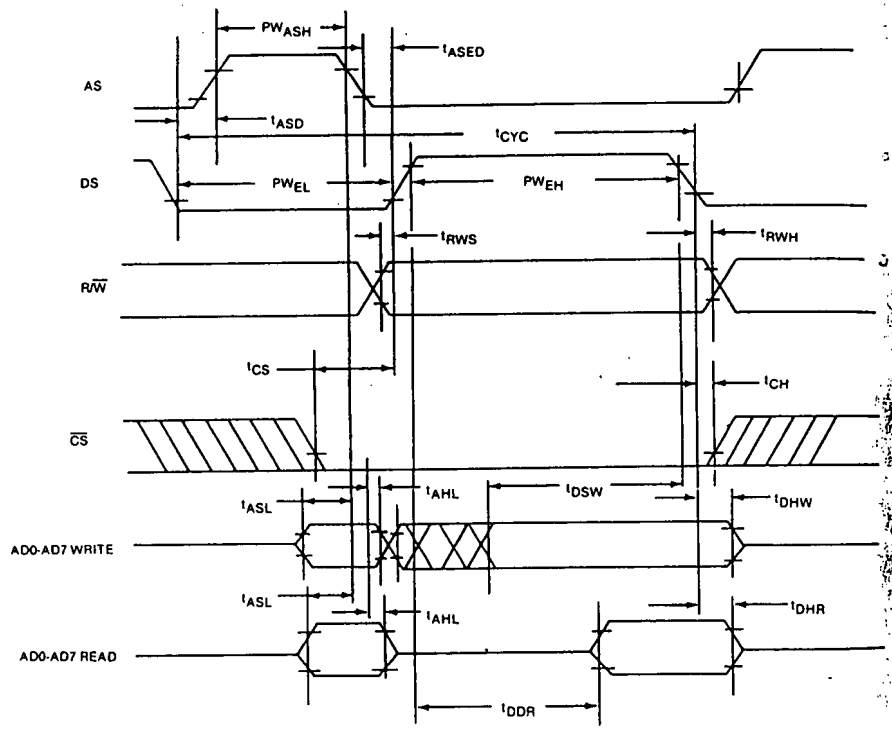
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4

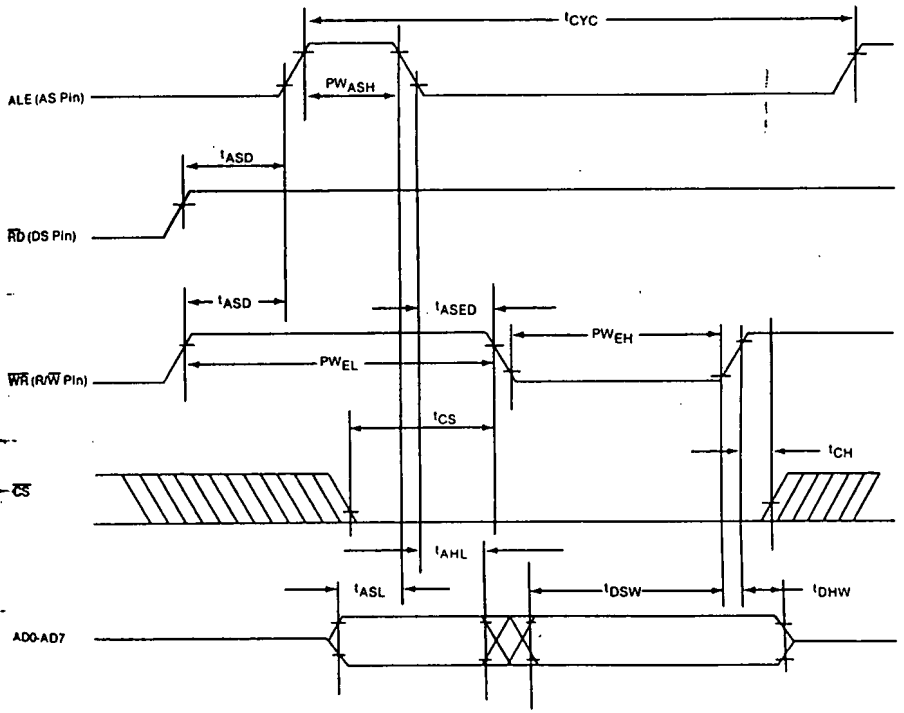


DS1287 BUS TIMING FOR MOTOROLA INTERFACE



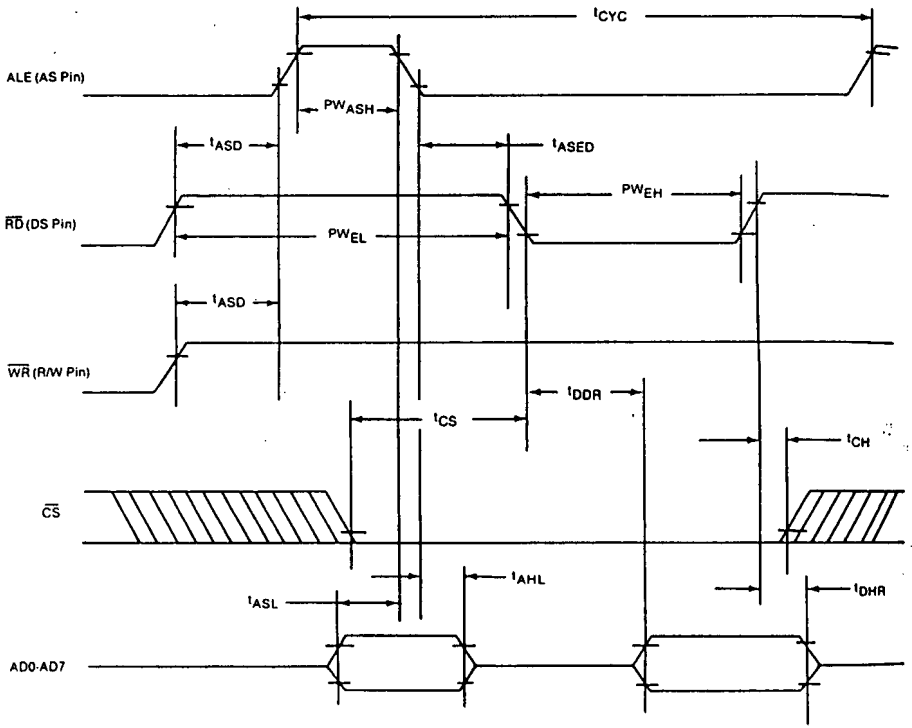
NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



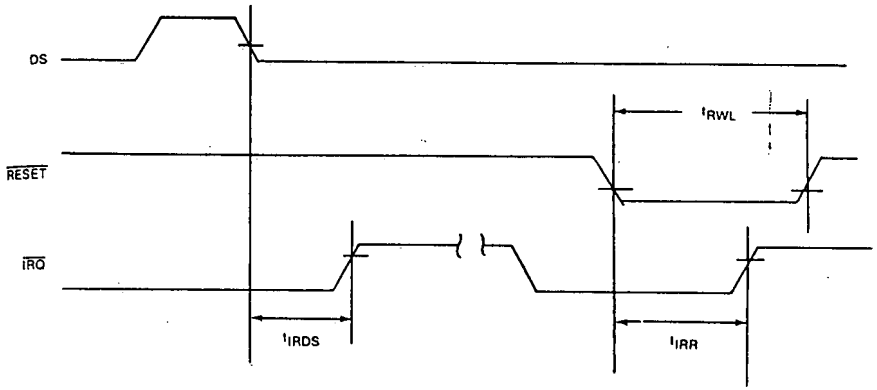
NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

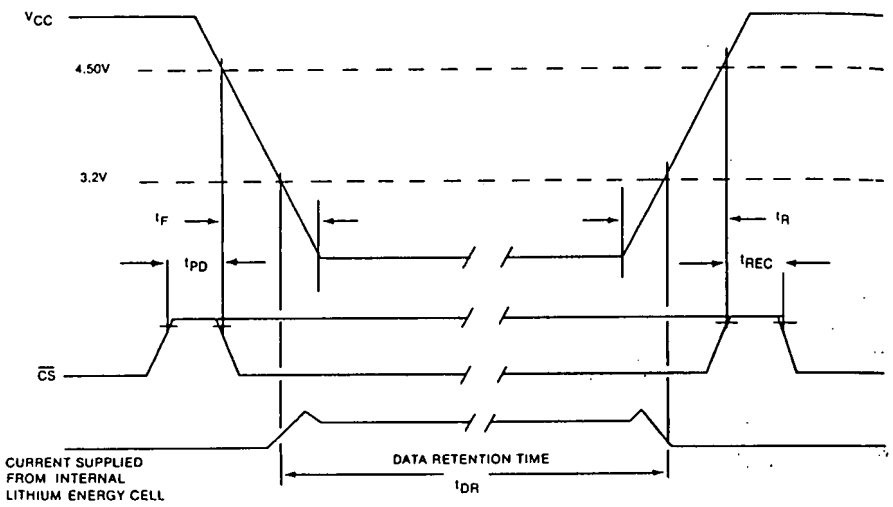
DS1287 IRQ RELEASE DELAY TIMING



NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

7

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

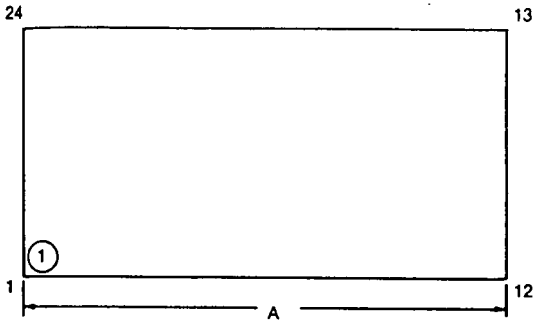
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		us	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		us	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	100		us	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	20	200	ms	

(t_A = 25°C)

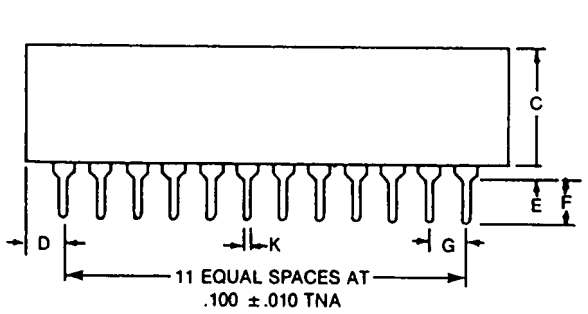
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention	10		years	

NOTE:
The real time clock will keep time to an accuracy of ± 1 minute per month during data retention time for the period of t_{DR}.

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.335
B	.685	.700
C	.345	.360
D	.100	.120
E	.015	.030
F	.110	.130
G	.090	.110
H	.590	.620
J	.008	.012
K	.015	.021



NOTE: Pins 2, 3, 16, 20, 21 and 22 are missing by design.

EXHIBIT E

ıalog
ɔlicating
mperature
ɔntrollers

ıeld Kits for Ranges and Options

OFF and time proportional
ı accuracy: ±2% of span
eatability: ±.1% of span
ıpact and versatile
3-mode PID option
V dc recorder output
cates the setpoint and
ıal process temperature

log Indicating Models I921 and I922

ɔ1 and I922 Controllers combine solid state cy with low cost. The I921 has a single set point ɔ I922 has two. They feature an easy-to-read dial ull 250° (angular) indicating meter and time ɔional control adjustable to true ON/OFF. Standard s on the I921 and I922 models include a plug-in 10 lay, isolated wiring chamber, either 115 or c operation (field convertible) and push-to-engage nt. The I922 additionally features either a tracking ard) or non-tracking second set point. The I921 and e available in J, K and T thermocouple calibrations, broad selection of ranges covering −350° to . Both models have a red LED indication of the relay status. The I922 also has a green LED for of the secondary relay.

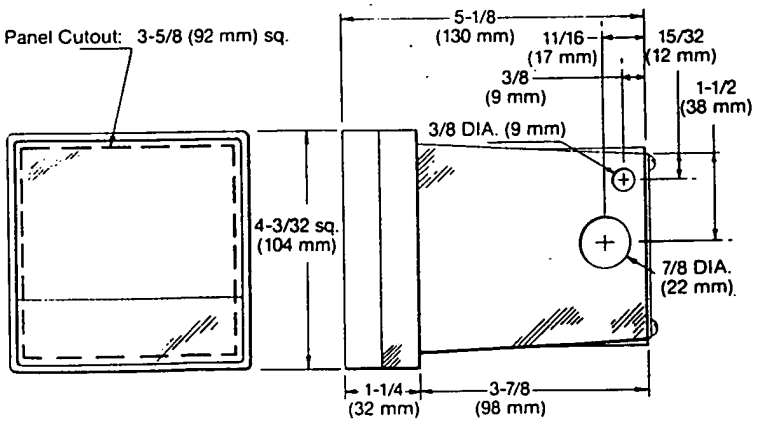
rsatile I921 and I922 models, as with all the Series ɔntrollers, are available with a wide variety of al control modes and switching devices. These ɔs are available as either factory-installed options or ɔ-install field kits. The optional switching devices e 15 amp solid state relays and a 4 to 20 mA tional control output. Control modes available e burst proportioning, high or low limit with reset , isolated 4 to 20 mA signal or full 3-mode rtional-integral-derivative (PID) control (I921 only) ither mechanical or solid state relays.

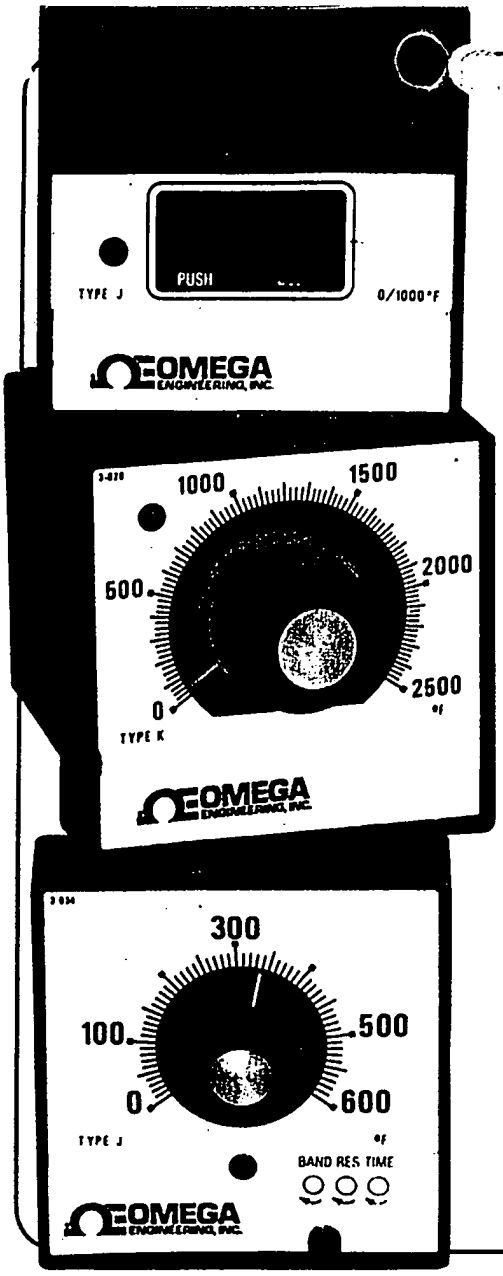
ɔ21 and I922 Controllers are available in many s and 3 thermocouple types to satisfy all rature control applications. These units are field rtible to another range or thermocouple type with the easy-to-install range kits. These kits increase rsatility of the I921 and I922 by allowing the user to change the range or thermocouple calibration as his requirements change. The kits include a custom range chip and self-adhesive dial. Only a screwdriver is required for the conversion. For a complete listing of all ranges and kits available for the I921 and I922 Controllers, see pages P-63 and P-65.

For ordering information, See Page P-66

$285
(1921 Single Set Point)

$345
(I922 Dual Set Point)





SPECIFICATIONS

Panel Cutout: 3⅝" (92 mm) sq. per DIN-43700

INPUTS

Thermocouples: Types J, K, T cold junction compensation.

- Standard upscale break protection, field convertible to downscale
- Lead Resistance: 1°F shift per 100 ohms.
- Interchangeability: range chips permit interchange of any standard analog thermocouple range.

MODES/SIGNAL FORMS

Time Proportioning to On/Off:

- Cycle time: adjustable approximately 2-36 sec.
- Bandwidth: adjustable 0-10% of span, with set point in the center.
- Manual Reset: adjustable ± 12% of span
- Field convertible to on-off mode with differential approximately .25% of span, symmetrical around set point.

Burst Proportioning:

- Same as time proportioning except cycle time adjustable approximately 0.2 to 3.6 sec. (Not for use with 10 amp relay.)

PID:

- Proportional-Integral-Derivative (3 modes).
- Internal jumpers allow selection of integral between 0 and .4 repeats per minute and derivative between 0 and 3 cycles per second.

4-20 mA (Isolated):

- 20 mA at lower end of proportional bandwidth, approximately 12 mA at set point, 4 mA at upper end of bandwidth. Bandwidth adjustable 0 to 6% of range span with set point in the center. Isolated optically and by transformer.

SWITCHING DEVICES

10 amp Mechanical Relay:

- Plug-in for easy replacement.
- Rated 10 amp @ 115V ac resistive, 5 amp at 240V ac resistive. SPDT.

1.5 amp Solid State Relay (SPST):

- Rated 1.5 amps @ 130°F ambient temperature, resistive or inductive, 24 to 230V ac.
- Surge current 30 amps for one cycle. Typical off-state leakage current 6 mA, @ 230V ac.
- Zero crossing, optically isolated.

15 amp Solid State Relay (SPST):

- Rated 15 amps @ 130°F ambient temperature, resistive or inductive 24 to 230V ac.
- Surge current 200 amps for one cycle. Typical off-state leakage current 6 mA, @ 230V ac.
- Zero crossing, optically isolated.
- Plugs into controller back and increases depth 1⅞".

High or Low Limit Modes with Reset Switch (10 amp mechanical relay required.)

- Available with primary or secondary outputs.
- Lock out on rising (falling) temperature.
- Manual reset switch.

Output Inversion

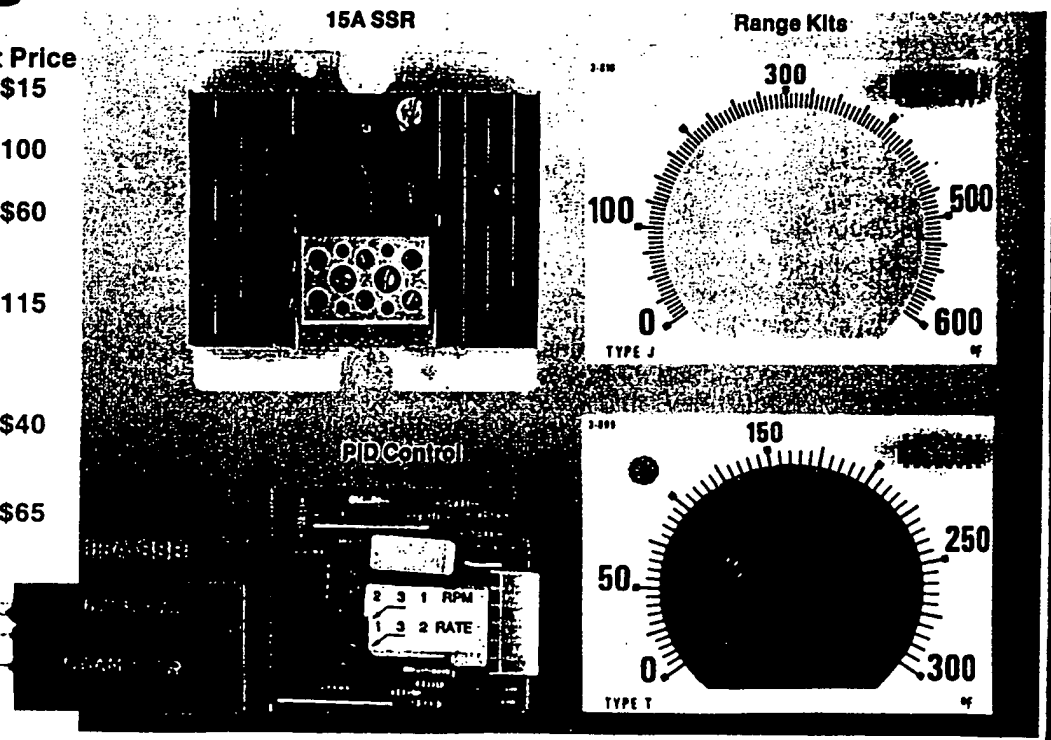
- For cooling applications.
- Available with solid state or mechanical relay.
- Failsafe control during power failure.

Nontracking Second Output

- Independent of primary set point.
- Adjustable over 100% of span.

PLUG-IN FIELD KITS

	List Price
KIT #62150-1 Mounting bracket	$15
KIT #62150-2 4-20 mA isolated (Model I921)	$100
KIT #62150-4 1.5 amp solid state relay, 24-230 V ac, zero crossing	$60
KIT #62150-5 15 amp solid state relay for plug-in to back of enclosure	$115
KIT #62150-6 Burst proportioning .2 to 3.6 sec. cycle time	$40
KIT #62150-7 Automatic Reset/Integral and Derivative (PID)	$65
Replacement Part 62138-61 Standard 10 amp electro-mech-relay	$15
KIT #62150-8 0-24 V dc switched output	$25

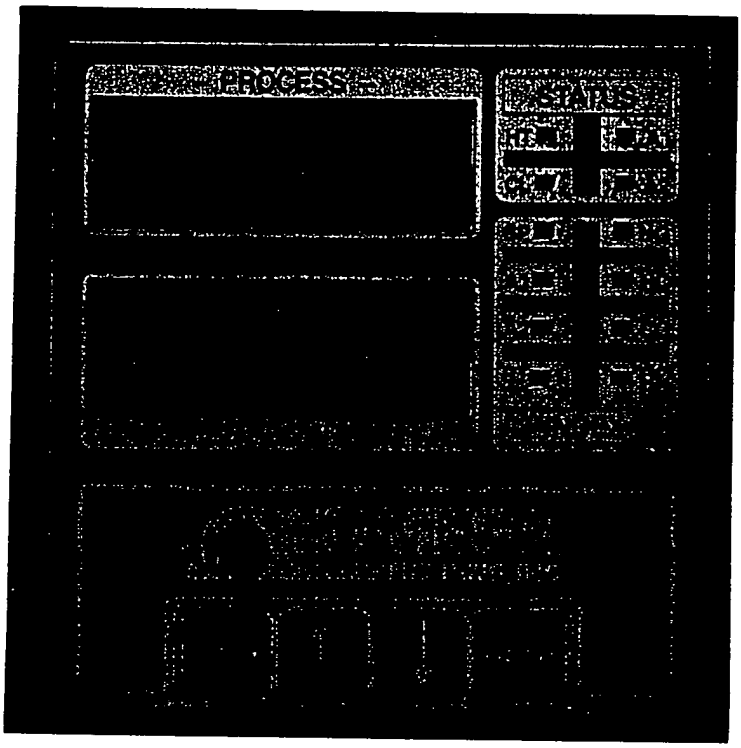


630

MICROPROCESSOR BASED TEMPERATURE CONTROLLER

Model 6000

- Heating and Cooling Outputs
- Dual 4-Digit Display
- Dual Process or Deviation Alarms
- Easy Touch-key Setup
- Compact—¼ DIN Case
- Only 3⅝" Deep



The Model 6000 Microprocessor-Based Controller provides the latest in heating and cooling control. A large dual 4-digit display shows process and set point temperatures at a glance. Three mode (proportional, integral and derivative) action eliminates offset as cooling and heating requirements change.

Touch-key setup eliminates all external knobs and protruding switches. Parameters are entered easily and can be locked in to prevent unauthorized tampering.

Heating and cooling outputs can be either relay, 4-20 mA, Triac or 20 V dc pulsed, in any combination.

Available with thermocouple types J, K or T, or RTD inputs, and ranges up to 2500°F (1370°C).

Thermocouple
Model 6001
Single Set Point
Single Output
(Heat Only)

From

$446

Thermocouple
Model 6002
Single Set Point
Dual Outputs
(Heat/Cool)

From

$483

nplete
: of
e Probes
your
Section J.

631

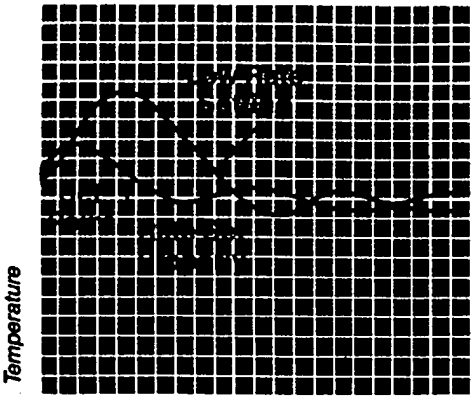
Microprocessor Based Temperature Controller

Model 6000

2 YEAR WARRANTY

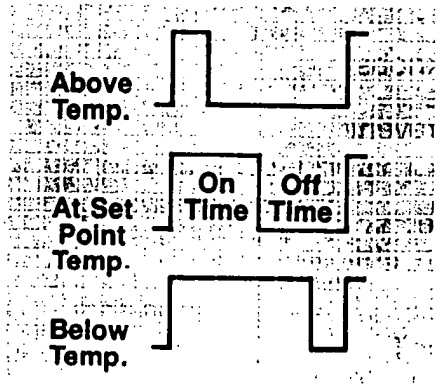
RATE WITH AUTOMATIC RESET

The rate function provides the controller with the ability to compensate for rapid changes in temperature. This function senses the rate of change, and applies immediate corrective action. Automatic reset, which tracks the rate, is used to eliminate offset (the difference between the set point and the stable process temperature). Using an integrator circuit, reset shifts the proportional band of the controller to correct for offset.



HEATING AND COOLING CYCLE TIMES

Adjustment of the cycle times for both the heater and cooler are required to match the controller to the process. Cycle times should be set to the longest possible, depending on the process, for increased relay life.
For the heater, the amount of power applied is increased below set point, and decreased above set point.
For the cooler, the amount of power applied is decreased below set point, and increased above set point.



PID CONTROL

OMEGA's unique Model 6000 microprocessor based controller was developed to satisfy the need of actual end users. Three mode (Proportional, Integral and Derivative) action eliminates offset (droop) as cooling and heating requirements change in the process and provides fast output response to rate of change and reduces temperature overshoot and undershoot.

The precision of the set point control is especially valuable because it produces more efficient operation, reduced reject rates and increased product quality.

TOUCH-KEY SETUP

All controls, parameters and function selections are entered at the touch of a key. All external knobs and switches have been eliminated. The completely digital controls can be indexed by touching one button, values can be adjusted at another touch and another touch enters the value. Once values are entered, they can be locked in with an internal switch to prevent unauthorized tampering.

THERMOCOUPLE LINEARIZATION

To assure accurate tracking between the display and the thermocouple, a precision program to linearize signal input from the thermocouple is programmed in the microprocessor. Linearization allows for more precise control and full use of the controllers range.

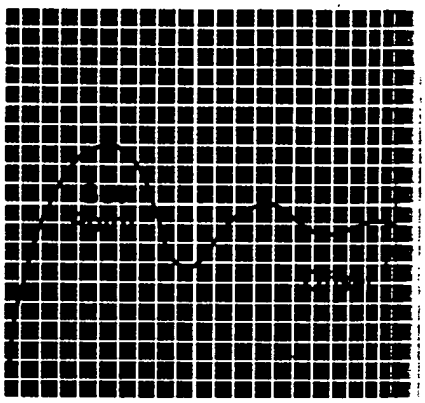
Dual Indication

Now you can compare process temperature and set point at a glance—hands free. The dual digital display concept has formerly only been available in high priced multifunction process controls.

HEAT AND COOL GAINS

Gains set the controller for proportional control of the heating and cooling actions. Gain is the change in control action required for a change in the process temperature. It is usually expressed in terms of the proportional bandwidth. Within the proportional band, the controller cycles on and off to control the process temperature. Below the band, heating action is at 100% (always on), and cooling action at 0% (always off). Above the band the heater is always off, and the cooler always on.

$$\text{Bandwidth (in degrees)} = \frac{\text{Full Scale Span (in degrees)}}{\text{Gain}}$$

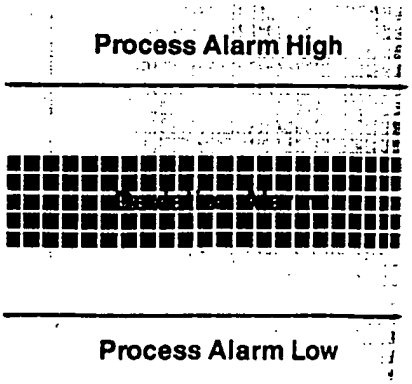


PROCESS OR DEVIATION ALARM

The process alarm will trip when the temperature is greater than the set point when configured as a high alarm.

It will trip when less than the setpoint when configured as a low alarm.

The deviation alarm will trip when the alarm setting is added (high) or subtracted (low) to the set point.



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Microprocessor-Based Process Controllers

CARE 2 YE
WARRA

- Thermocouple, F Process Voltage Current Input
- Relay, SSR Drive 4-20 mA Output
- On-Off, Proportic and Autotune PI
- Sealed Faceplate Wash-Down Environments
- Less Than 4" Pa Depth
- 85 to 265 Vac Po
- Inoperative Heat Available

CN4400 Series
1/16 DIN Size
$190
Page P-34

CN4500 Series
1/8 DIN Size
$300
From
Page P-35

Transition Joint Probes sold separately, page A-6.

CN4700 Series
72 mm Square DIN Size
$350
Page P-35

Shown Actual

CN4600 Series
1/4 DIN Size
From **$30**
Page P-35

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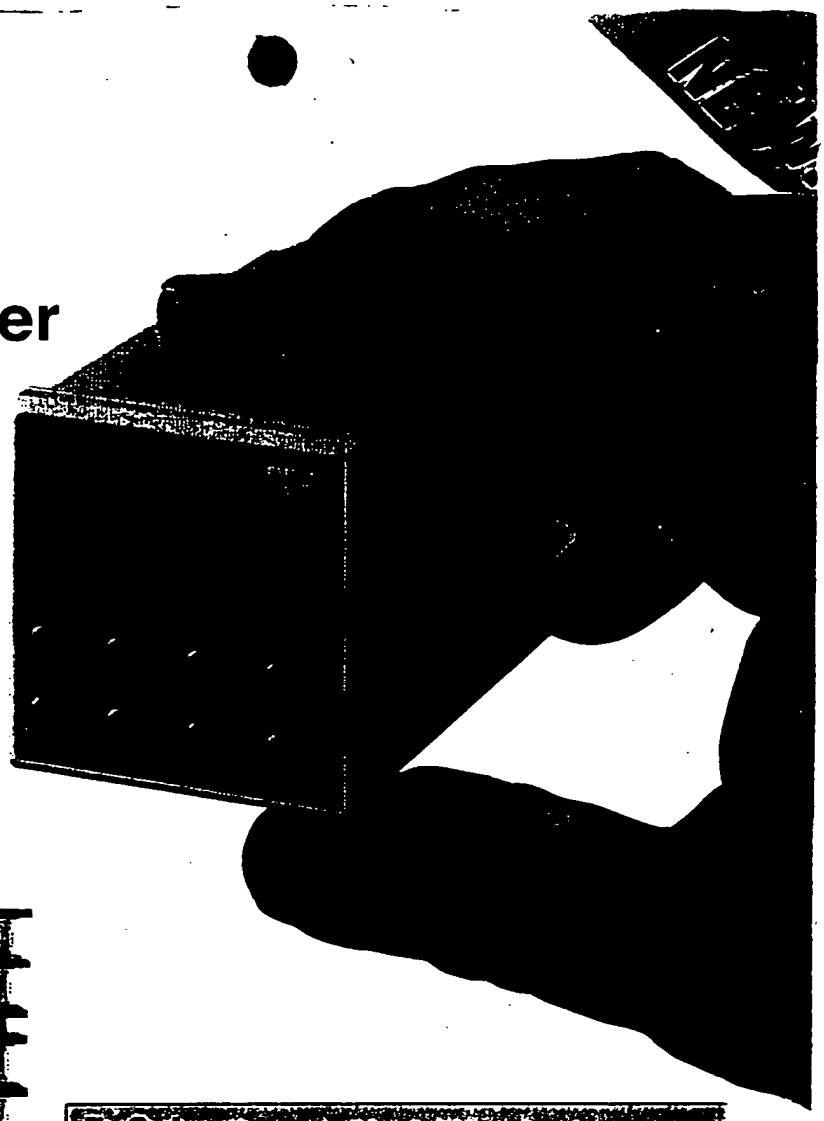
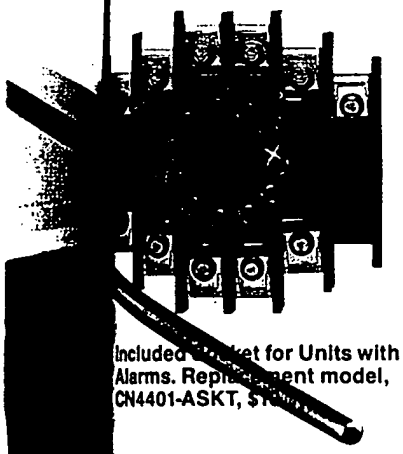
1/16 DIN Micro Controller

The CN4400 is an economical 1/16 DIN process controller that accepts temperature or process inputs. It has sophisticated control capabilities, providing PID, autotune PID and on-off control. The CN4400 is available with mechanical relay, SSR driver or 4-20 mA output. For fast hook-up, the CN4400 features a removeable socket mount design with screw terminals.

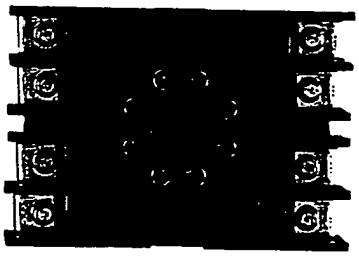
CN4400 Series

$190





Included Socket for Units with Alarms. Replacement model, CN4401-ASKT, $10.



Included Socket for Units without Alarms. Replacement model, CN4401-SKT, $10.

To Order (Specify Model Number)		
Model No.	**Price**	**Description**
CN4401TR	$190	Thermocouple or RTD input
CN4401CV	190	1-5 Vdc/4-20 mA input

Each unit includes mounting socket.

Input Types and Ranges – All CN4000 Units

Input Code	Type	Range °F	Range °C
TR	J	32 to 1832	0 to 1000
	K	32 to 2192	0 to 1200
	T	–328 to 752	–200 to 400
	E	32 to 1472	0 to 800
	R	32 to 2912	0 to 1600
	S	32 to 2912	0 to 1600
	B	32 to 3212	0 to 1800
	RTD	–238 to 752	–150 to 400
CV	V	1 to 5 Vdc	
	mA	4 to 20 mA dc	

Output Types and Options

Ordering Suffix	Add'l Price	Description
(std)	N/C	Standard Mechanical Relay Output, 3 A (SPDT)
-D	$25	Optional SSR Driver Output, 24 Vdc
-F	N/C	Optional 4-20 mA Output
-A	25	Optional single 1 A (SPST) Alarm Relay

Output Types – All CN4000 Units

Type	Description
Mechanical Relay	SPDT, Rated 3 A @ 220 Vac
SSR Driver	24 Vdc Pulse
Current	4-20 mA dc <600Ω load resistance

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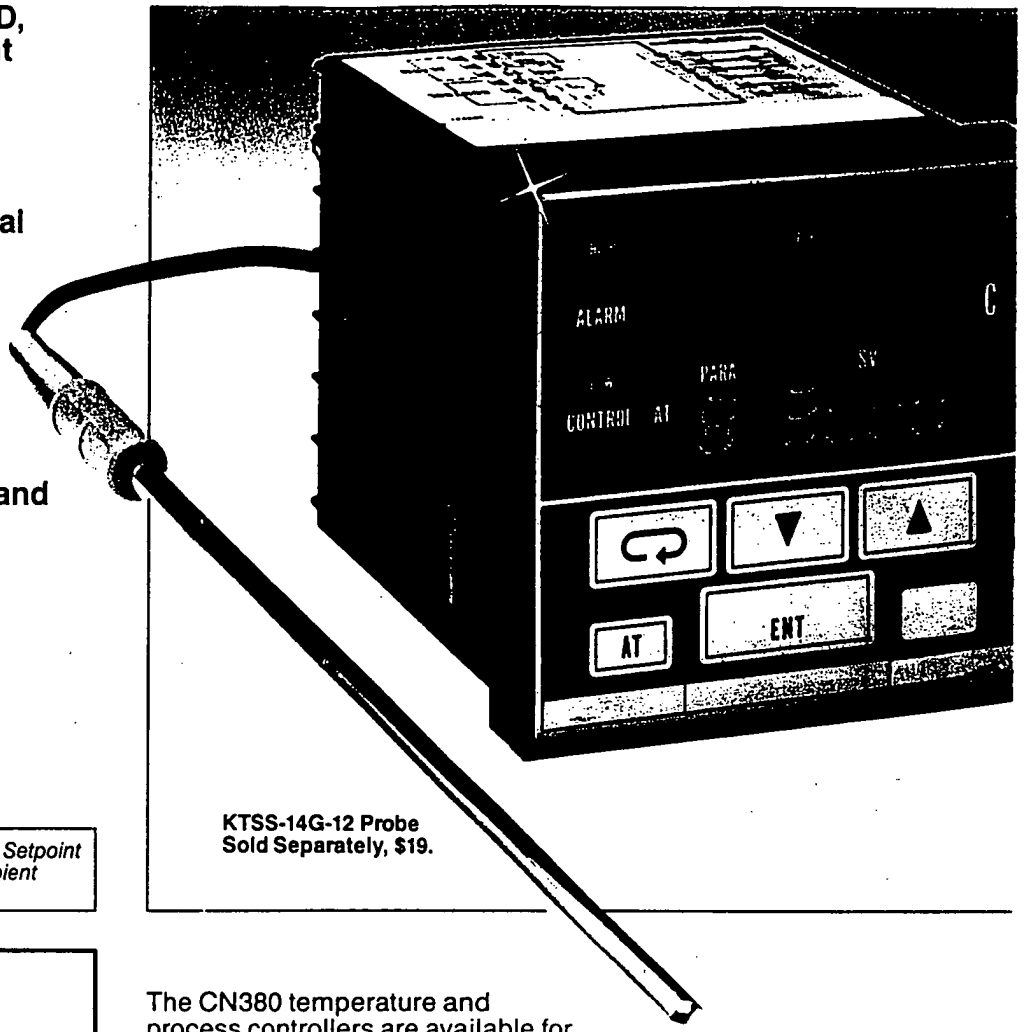
Temperature PID Controller
Auto and Manual Tuning

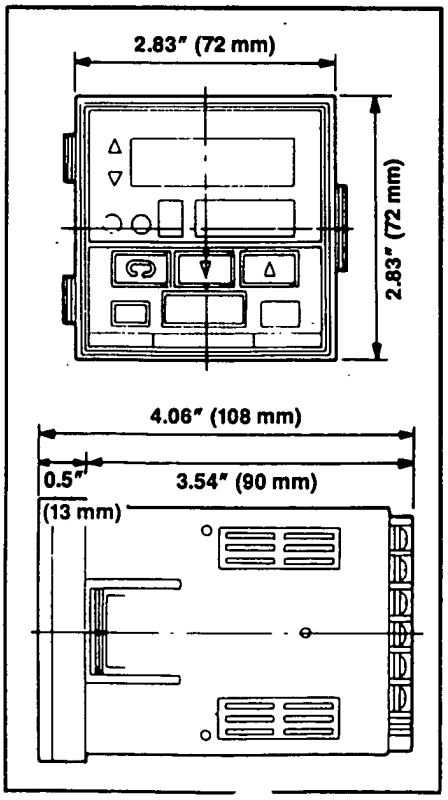
- Thermocouple, RTD, Voltage and Current Input Models
- Relay, SSR Driver, Voltage or Current Output Models
- Automatic or Manual Tuning on Demand
- Compact Size with 2.7" Square Cutout
- Optional Alarms Selectable for Process/Deviation Action
- Isolation of Inputs and Outputs



KTSS-14G-12 Probe
Sold Separately, $19.

CN380 Series
$299

For Best Results with Auto-Tuning, Setpoint Should be at Least 100° Over Ambient Temperature



The CN380 temperature and process controllers are available for thermocouple, RTD, voltage or current input. Thermocouple and RTD input models allow the user to select from 11 thermocouple types, or 2 RTD curves. Voltage and current input models allow user-programmable scaling within the −1999 to 7999 count range; the minimum span is 100 counts, while the max. is 5000 counts.

The CN380 features PID auto-tuning for automatic selection of the optimum PID values, or manual setting of the PID parameters. The CN380 is available with either mechanical relay, dc SSR driver, proportional voltage or current outputs. Relay and SSR driver output models can also provide on/off control, if desired.

The optional alarm package offers two alarm points that can be set to any values within the sensor range. These setpoints can be set to absolute or deviation alarms.

Program features also include a keylock for preventing tamperin

To Order (Specify Model N

Model No.	Price	Output Type
CN381(*)	$299	mechanical
CN382(*)	299	SSR driver
CN383(*)	299	4-20 mA cur
CN384(*)	299	0-10 Vdc Vol

Specify Input type:
TC — Thermocouple
RTD — Pt RTD, 3-wire, 100 ohm
MV — voltage to 50 mVdc
V — voltage to 5 Vdc
MA — current to 20 mA

Options

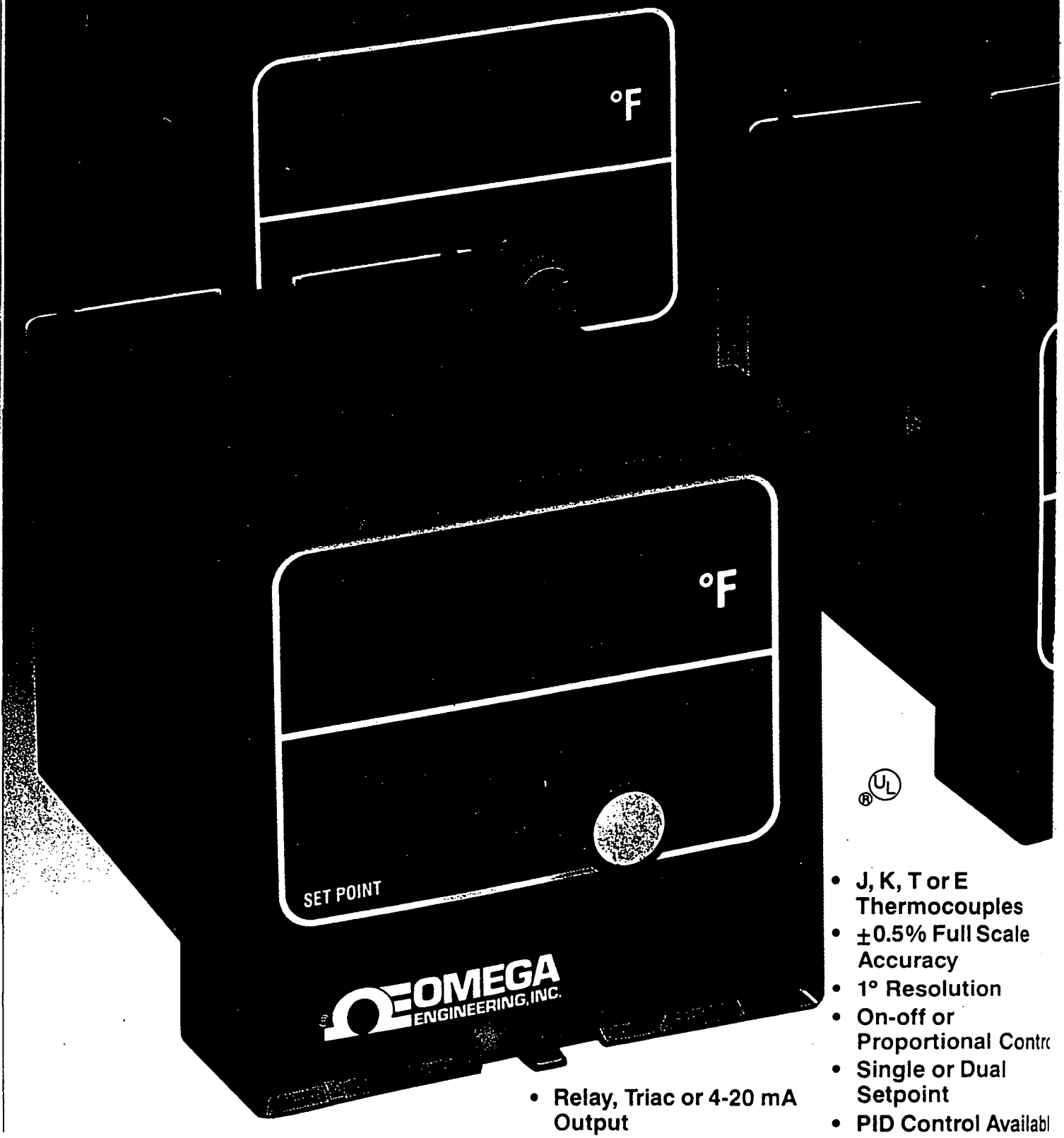
Ordering Suffix	Add'l Cost	Description
-A	$50	Dual Alarm

Ordering Example: *CN381TC-A, $349. CN380 controller, with thermocouple inp and mechanical relay output, and dual a*

635

Digital Temperature Controllers
CN5000 Series

~~USA~~

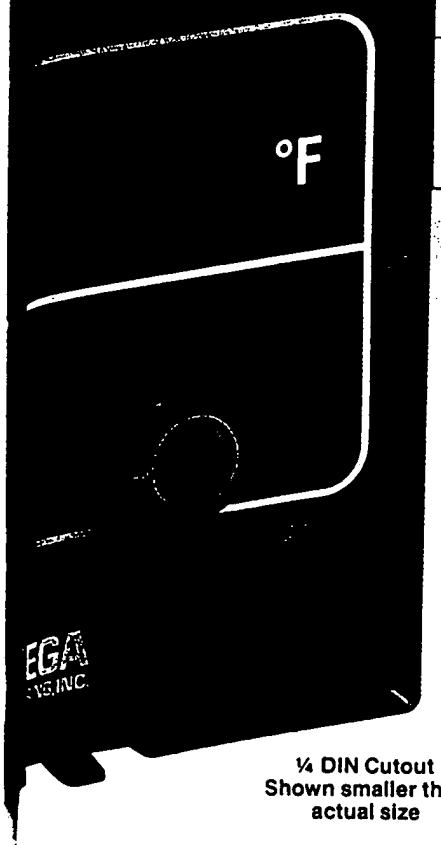


- J, K, T or E Thermocouples
- ±0.5% Full Scale Accuracy
- 1° Resolution
- On-off or Proportional Contr
- Single or Dual Setpoint
- PID Control Availabl
- Relay, Triac or 4-20 mA Output

636

Input Type	Range	No. of Outputs	Model Number	Price
J Iron Constantan	0 to 650°C	Single	CN5001J1	$295
		Dual	CN5002J1	345
	0 to 1000°F	Single	CN5001J2	295
		Dual	CN5002J2	345
K Chromel Alumel	0 to 2000°F	Single	CN5001K1	345
	0 to 1000°C	Single	CN5001K2	295
		Dual	CN5002K2	345
	0 to 1000°F	Single	CN5001K3	295
		Dual	CN5002K3	345
T Copper Constantan	0 to 350°C	Single	CN5001T1	295
		Dual	CN5002T1	345
	0 to 650°F	Single	CN5001T2	295
		Dual	CN5002T2	345
	−85 to 350°C	Single	CN5001T3	295
		Dual	CN5002T3	345
E Chromel Constantan	0 to 650°C	Single	CN5001E1	295
		Dual	CN5002E1	345
	0 to 1000°F	Single	CN5001E2	295
		Dual	CN5002E2	345

IN STOCK FOR FAST DELIVERY



¼ DIN Cutout
Shown smaller than actual size

2 YEAR WARRANTY

From
$285

The OMEGA® CN5000 Series Digital Controllers are designed for maximum versatility at an economical price. These units have standard features including a 10 amp mechanical relay with either proportional or on/off control, an easy-to-read LED display, push-to-engage setpoint knob, and LED indication of output status. J, K, T or E thermocouple types may be used as input, with either Celsius or Fahrenheit display.

The modular design of these controllers enables them to be used in various applications. These optional control modes and outputs are also available as field installable kits. Various output types include solid state relay and 4-20 mA proportional current. PID control is also available, with either relay or current output.

Model CN5001 Single Setpoint Proportional and On-Off Controller

$295

This versatile digital controller can be operated as either a proportional or on-off controller. Set the adjustable bandwidth at up to 10% of full scale and it's a proportional controller. Or, with the bandwidth set to 0, on-off control with a 0.25% of span differential is possible. To read and adjust the setpoint, simply depress the push-to-set knob, and turn it to the desired setpoint.

The standard CN5001 is available with either J, K, T or E thermocouple types, and has a 10 A mechanical relay. Available options include solid state relays or proportional current outputs, and PID (proportional-integral-derivative) control. For information on ordering models with control, output and other options, see page P-53.

Model CN5002 Dual Setpoint Controller

$345

The first setpoint of the CN5002 incorporates the features of the CN5001 with the addition of an independent second setpoint and output. The second setpoint temperature may be set to any value within the full span of the controller, independent of the first setpoint. The second setpoint has an ON-OFF control, and a blind adjustment. For ordering information of non-standard models, see page P-53.

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EXHIBIT F

Reference Temperatures

We cannot build a temperature divider as we can a voltage divider, nor can we add temperatures as we would add lengths to measure distance. We must rely upon temperatures established by physical phenomena which are easily observed and consistent in nature. The International Practical Temperature Scale (IPTS) is based on such phenomena. Revised in 1968, it establishes eleven reference temperatures.

Since we have only these fixed temperatures to use as a reference, we must use instruments to interpolate between them. But accurately interpolating between these temperatures can require some fairly exotic transducers, many of which are too complicated or expensive to use in a practical situation. We shall limit our discussion to the four most common temperature transducers: thermocouples, resistance-temperature detector's (RTD's), thermistors, and integrated circuit sensors.

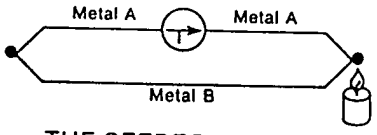
IPTS-68 REFERENCE TEMPERATURES

EQUILIBRIUM POINT	K	°C
Triple Point of Hydrogen	13.81	−259.34
Liquid/Vapor Phase of Hydrogen at 25/76 Std. Atmosphere	17.042	−256.108
Boiling Point of Hydrogen	20.28	−252.87
Boiling Point of Neon	27.102	−246.048
Triple Point of Oxygen	54.361	−218.789
Boiling Point of Oxygen	90.188	−182.962
Triple Point of Water	273.16	.01
Boiling Point of Water	373.15	100
Freezing Point of Zinc	692.73	419.58
Freezing Point of Silver	1235.08	961.93
Freezing Point of Gold	1337.58	1064.43

Table 1

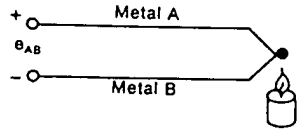
THE THERMOCOUPLE

When two wires composed of dissimilar metals are joined at both ends and one of the ends is heated, there is a continuous current which flows in the *thermoelectric* circuit. Thomas Seebeck made this discovery in 1821.



THE SEEBECK EFFECT
Figure 2

If this circuit is broken at the center, the net open circuit voltage (the Seebeck voltage) is a function of the junction temperature and the composition of the two metals.



e_{AB} = SEEBECK VOLTAGE
Figure 3

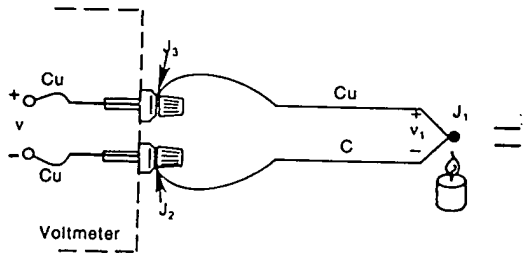
All dissimilar metals exhibit this effect. The most common combinations of two metals are listed in Appendix B of this application note, along with their important characteristics. For small changes in temperature the Seebeck voltage is linearly proportional to temperature:

$$\Delta e_{AB} = \alpha \Delta T$$

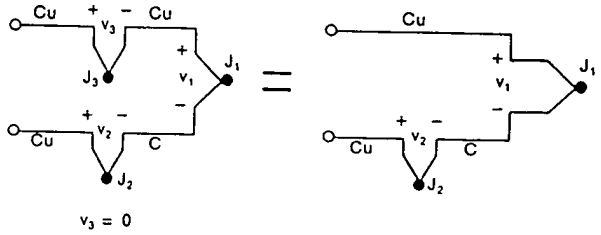
Where α, the Seebeck coefficient, is the constant of proportionality.

Measuring Thermocouple Voltage – We can't measure the Seebeck voltage directly because we must first connect a voltmeter to the thermocouple, and the voltmeter leads themselves create a new thermoelectric circuit.

Let's connect a voltmeter across a copper-constantan (Type T) thermocouple and look at the voltage output:



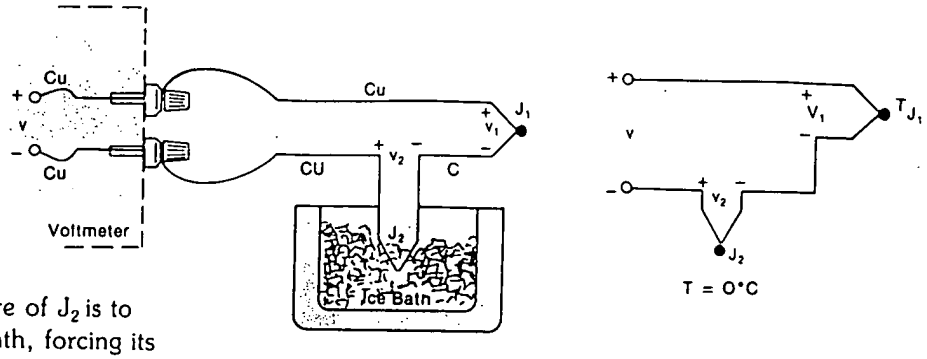
EQUIVALENT CIRCUITS:



$V_3 = 0$

MEASURING JUNCTION VOLTAGE WITH A DVM
Figure 4

We would like the voltmeter to read only V_1, but by connecting the voltmeter in an attempt to measure the output of Junction J_1, we have created two more metallic junctions: J_2 and J_3. Since J_3 is a copper-to-copper junction, it creates no thermal EMF ($V_3 = 0$) but J_2 is a copper-to-constantan junction which will add an EMF (V_2) in opposition to V_1. The resultant voltmeter reading V will be proportional to the temperature *difference* between J_1 and J_2. This says that we can't find the temperature at J_1 unless we first find the temperature of J_2.



EXTERNAL REFERENCE JUNCTION
Figure 5

One way to determine the temperature of J_2 is to physically put the junction into an ice bath, forcing its temperature to be 0°C and establishing J_2 as the *Reference Junction*. Since both voltmeter terminal junctions are now copper-copper, they create no thermal emf and the reading V on the voltmeter is proportional to the temperature difference between J_1 and J_2.

Now the voltmeter reading is (See Figure 5):

$$V = (V_1 - V_2) \cong \alpha\,(t_{J_1} - t_{J_2})$$

If we specify T_{J_1} in degrees Celsius:

$$T_{J_1}\,(°C) + 273.15 = t_{J_1}$$

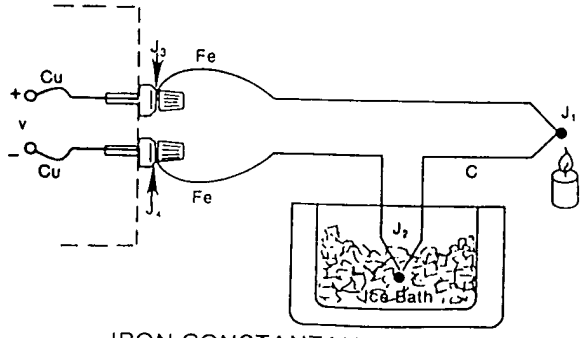
then V becomes:

$$V = V_1 - V_2 = \alpha\,[(T_{J_1} + 273.15) - (T_{J_2} + 273.15)]$$
$$= \alpha\,(T_{J_1} - T_{J_2}) = \alpha(T_{J_1} - 0)$$
$$V = \alpha T_{J_1}$$

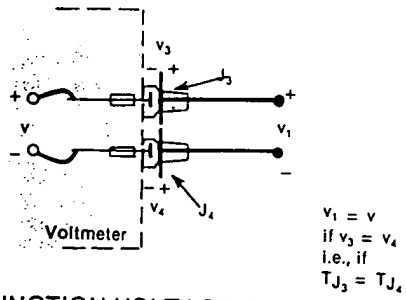
We use this protracted derivation to emphasize that the ice bath junction output, V_2, is *not* zero volts. It is a function of absolute temperature.

By adding the voltage of the ice point reference junction we have now referenced the reading V to 0°C. This method is very accurate because the ice point temperature can be precisely controlled. The ice point is used by the National Bureau of Standards (NBS) as the fundamental reference point for their thermocouple tables, so we can now look at the NBS tables and directly convert from voltage V to Temperature T_{J_1}.

The copper-constantan thermocouple shown in Figure 5 is a unique example because the copper wire is the same metal as the voltmeter terminals. Let's use an iron-constantan (Type J) thermocouple instead of the copper-constantan. The iron wire (Figure 6) increases the number of dissimilar metal junctions in the circuit, as both voltmeter terminals become Cu-Fe thermocouple junctions.

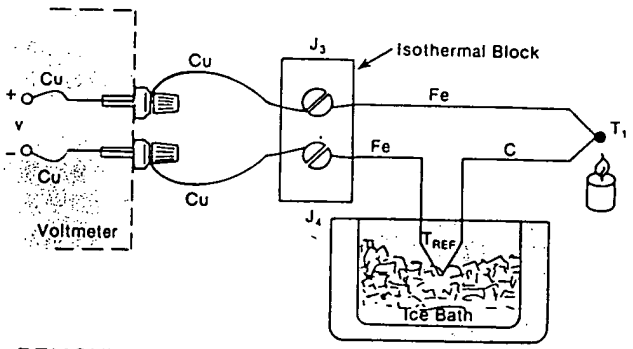


IRON-CONSTANTAN COUPLE
Figure 6



JUNCTION VOLTAGE CANCELLATION
Figure 7

If both front panel terminals are not at the same temperature, there will be an error. For a more precise measurement the copper voltmeter leads should be extended so the copper-to-iron junctions are made on an *isothermal* (same temperature) block:



REMOVING JUNCTIONS FROM DVM TERMINALS
Figure 8

The isothermal block is an electrical insulator but a good heat conductor and it serves to hold J_3 and J_4 at the same temperature. The absolute block temperature is unimportant because the two Cu-Fe junctions act in opposition. We still have

$$V = \alpha(T_1 - T_{REF})$$

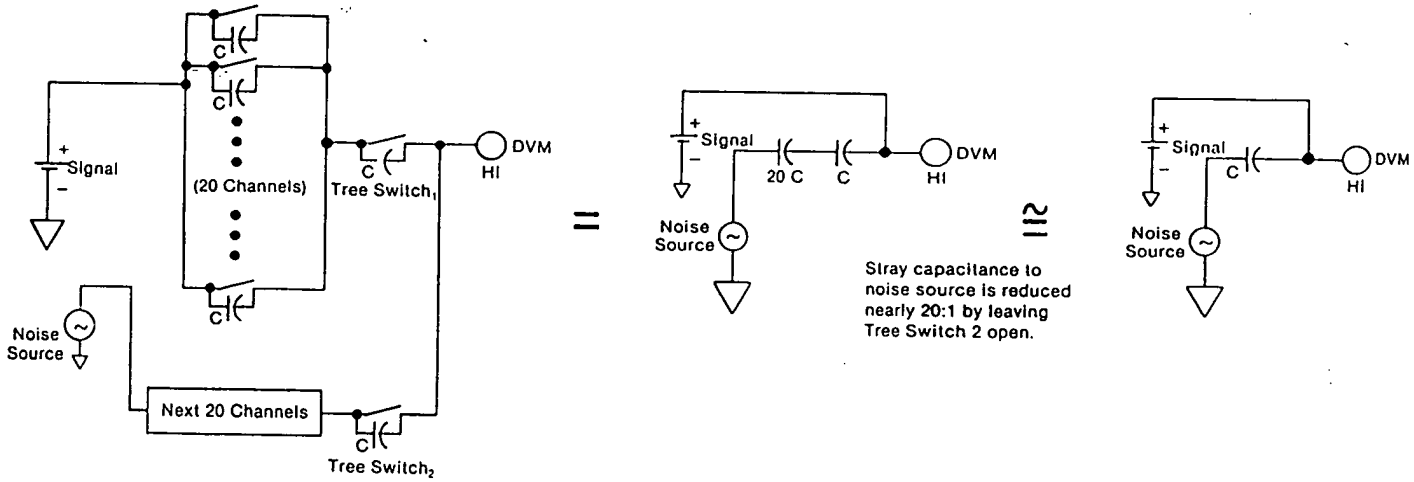
Noise Rejection

Tree Switching – Tree switching is a method of organizing the channels of a scanner into groups, each with its own main switch.

Without tree switching, every channel can contribute noise directly through its *stray* capacitance. With tree switching, groups of parallel channel capacitances are in series with a single *tree switch* capacitance. The result is greatly reduced crosstalk in a large data acquisition system, due to the reduced interchannel capacitance.

Guarding – Guarding is a technique used to reduce interference from any noise source that is common to both high and low measurement leads, i.e., from *common mode* noise sources.

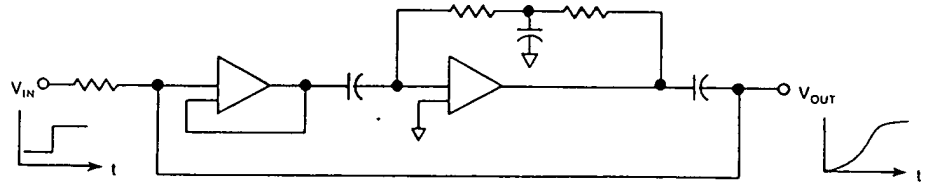
Let's assume a thermocouple wire has been pulled through the same conduit as a 220V AC supply line. The capacitance between the power lines and the thermocouple lines will create an AC signal of approximately equal magnitude on both thermocouple wires. This *common mode* signal is not a problem in an ideal



TREE SWITCHING
Figure 19

Analog Filter – A filter may be used directly at the input of a voltmeter to reduce noise. It reduces interference dramatically, but causes the voltmeter to respond more slowly to step inputs.

through the thermocouple lead resistance, creating a normal mode noise signal. The guard, physically a circuit, but the voltmeter is not ideal. It has some capacitance between its low terminal and safety ground (chassis). Current flows through this capacitance and floating metal box surrounding the entire voltmeter circuit, is connected to a shield surrounding the thermocouple wire, and serves to shunt the interfering current.



ANALOG FILTER
Figure 20

Integration – Integration is an A/D technique which essentially averages noise over a full line cycle, thus power line-related noise and its harmonics are virtually eliminated. If the integration period is chosen to be less than an integer line cycle, its noise rejection properties are essentially negated.

Since thermocouple circuits that cover long distances are especially susceptible to power line related noise, it is advisable to use an integrating analog to digital conveter to measure the thermocouple voltage. Integration is an especially attractive A/D technique in light of recent innovations which allow reading rates of 48 samples per second with full cycle integration.

through the thermocouple lead resistance, creating a normal mode noise signal. The guard, physically a floating metal box surrounding the entire voltmeter circuit, is connected to a shield surrounding the thermocouple wire, and serves to shunt the interfering current.

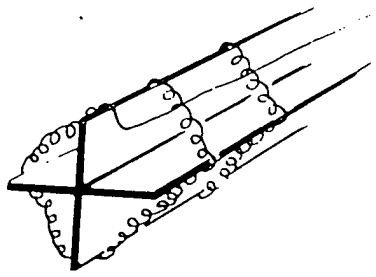
THE RTD

History

The same year that Seebeck made his discovery about thermoelectricity, Sir Humphrey Davy announced that the resistivity of metals showed a marked temperature dependence. Fifty years later, Sir William Siemens proffered the use of platinum as the element in a resistance thermometer. His choice proved most propitious, as platinum is used to this day as the primary element in all high-accuracy resistance thermometers. In fact, the Platinum Resistance Temperature Detector, or PRTD, is used today as an interpolation standard from the oxygen point (−182.96°C) to the antimony point (630.74°C).

Platinum is especially suited to this purpose, as it can withstand high temperatures while maintaining excellent stability. As a noble metal, it shows limited susceptibility to contamination.

The classical resistance temperature detector (RTD) construction using platinum was proposed by C.H. Meyers in 1932.[12] He wound a helical coil of platinum on a crossed mica web and mounted the assembly inside a glass tube. This construction minimized strain on the wire while maximizing resistance.



MEYERS RTD CONSTRUCTION
Figure 35

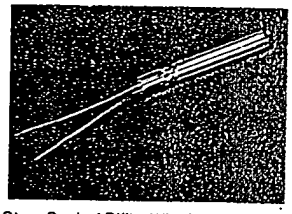
Although this construction produces a very stable element, the thermal contact between the platinum and the measured point is quite poor. This results in a slow thermal response time. The fragility of the structure limits its use today primarily to that of a laboratory standard.

Another laboratory standard has taken the place of the Meyer's design. This is the *bird-cage* element proposed by Evans and Burns.[16] The platinum element remains largely unsupported, which allows it to move freely when expanded or contracted by temperature variations.

Strain-induced resistance changes with time and temperature are thus minimized, and the bird-cage becomes the ultimate laboratory standard. Due to the unsupported structure and subsequent susceptibility to vibration, this configuration is still a bit too fragile for industrial environments.

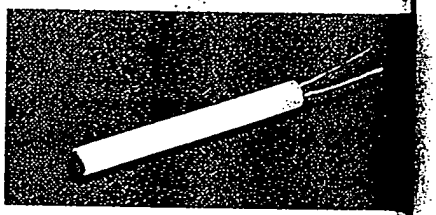
A more rugged construction technique is shown in Figure 37. The platinum wire is bifilar wound on a glass or ceramic bobbin. The bifilar winding reduces the effective enclosed area of the coil to minimize magnetic pickup and its related noise. Once the wire is wound onto the bobbin, the assembly is then sealed with a coating of molten glass. The sealing process assures that the RTD will maintain its integrity under extreme vibration, but it also limits the expansion of the platinum metal at high temperatures. Unless the coefficients of expansion of the platinum and the bobbin match perfectly, stress will be placed on the wire as the temperature changes, resulting in a strain-induced resistance change. This may result in a permanent change in the resistance of the wire.

There are partially supported versions of the RTD which offer a compromise between the bird-cage approach and the sealed helix. One such approach uses a platinum helix threaded through a ceramic cylinder and affixed via glass-frit. These devices will maintain excellent stability in moderately rugged vibrational applications.

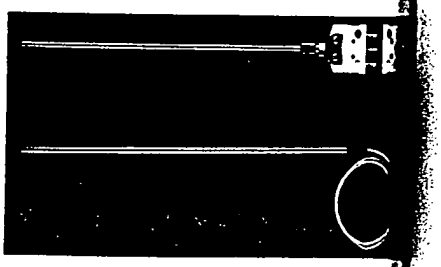


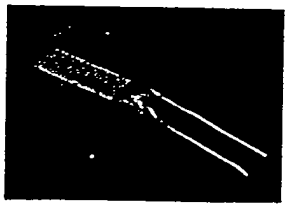
Glass Sealed Bifilar Winding

Thick Film Omega Film Element



Typical RTD Probes





Thin Film Omega TFD Element

TYPICAL RTDs
Figures 36 and 37

Metal Film RTD's

In the newest construction technique, a platinum or metal-glass slurry film is deposited or screened onto a small flat ceramic substrate, etched with a laser-trimming system, and sealed. The film RTD offers substantial reduction in assembly time and has the further advantage of increased resistance for a given size. Due to the manufacturing technology, the device size itself is small, which means it can respond quickly to step changes in temperature. Film RTD's are presently less stable than their hand-made counterparts, but they

[12] Refer to Bibliography 12.
[16] Refer to Bibliography 16.

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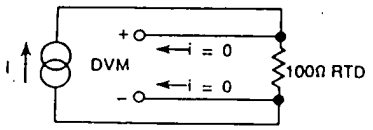
4-Wire Ohms – The technique of applying a current source along with a remotely sensed digital voltmeter alleviates many problems associated with the bridge.



4-WIRE OHMS MEASUREMENT
Figure 42

The output voltage read by the dvm is directly proportional to RTD resistance, so only one conversion equation is necessary. The three bridge-completion resistors are replaced by one reference resistor. The digital voltmeter measures only the voltage dropped across the RTD and is insensitive to the length of the lead wires.

The one disadvantage of using 4-wire ohms is that we need one more extension wire than the 3-wire bridge. This is a small price to pay if we are at all concerned with the accuracy of the temperature measurement.

3-Wire Bridge Measurement Errors

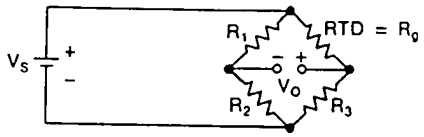


Figure 43

If we know V_S and V_O, we can find R_g and then solve for temperature. The unbalance voltage V_O of a bridge built with $R_1 = R_2$ is:

$$V_O = V_S \left(\frac{R_3}{R_3 + R_g}\right) - V_S \left(\frac{1}{2}\right)$$

If $R_g = R_3$, $V_O = 0$ and the bridge is balanced. This can be done manually, but if we don't want to do a manual bridge balance we can just solve for R_g in terms of V_O:

$$R_g = R_3 \left(\frac{V_S - 2V_O}{V_S + 2V_O}\right)$$

This expression assumes the lead resistance is zero. If R_g is located some distance from the bridge in a 3-wire configuration, the lead resistance R_L will appear in series with both R_g and R_3:

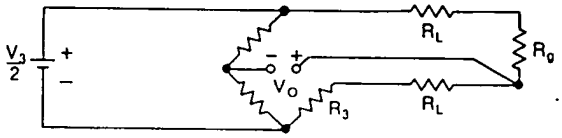


Figure 44

Again we solve for R_g:

$$R_g = R_3 \left(\frac{V_S - 2V_O}{V_S + 2V_O}\right) - R_L \left(\frac{4V_O}{V_S + 2V_O}\right)$$

The error term will be small if V_O is small, i.e., the bridge is close to balance. This circuit works well with devices like strain gauges, which change resistance value by only a few percent, but an RTD changes resistance dramatically with temperature. Assume the RTD resistance is 200 ohms and the bridge is designed for 100 ohms:

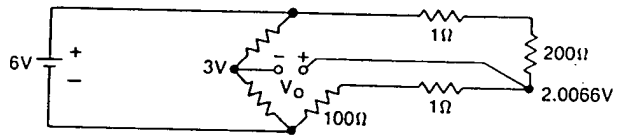


Figure 45

Since we don't know the value of R_L, we must use equation (a), so we get:

$$R_g = 100 \left(\frac{6 - 1.9868}{6 + 1.9868}\right) = 199.01 \text{ ohms}$$

The correct answer is of course 200 ohms. That's a temperature error of about 2½°C.

Unless you can actually measure the resistance of R_L or balance the bridge, the basic 3-wire technique is not an accurate method for measuring absolute temperature with an RTD. A better approach is to use a 4-wire technique.

Resistance to Temperature Conversion

The RTD is a more linear device than the thermocouple, but it still requires curve-fitting. The Callendar-Van Dusen equation has been used for years to approximate the RTD curve:[11, 13]

$$R_T = R_0 + R_0 \alpha \left[T - \delta\left(\frac{T}{100} - 1\right)\left(\frac{T}{100}\right) - \beta\left(\frac{T}{100} - 1\right)\left(\frac{T^3}{100}\right)\right]$$

Where:

R_T = Resistance at Temperature T
R_0 = Resistance at T = 0°C
α = Temperature coefficient at T = 0°C (typically +0.00392Ω/Ω/°C)
δ = 1.49 (typical value for .00392 platinum)
β = 0 T > 0
0.11 (typical) T < 0

The exact values for coefficients α, β, and δ are determined by testing the RTD at four temperatures and solving the resultant equations. This familiar equation was replaced in 1968 by a 20th order polynomial

[11, 13] Refer to Bibliography 11 and 13.

Introduction to pH

INTRODUCTION

pH is a unit of measure which describes the degree of acidity or alkalinity of a solution. It is measured on a scale of 0 to 14. The term pH is derived from "p", the mathematical symbol of the negative logarithm, and "H", the chemical symbol of Hydrogen. The formal definition of pH is the negative logarithm of the Hydrogen ion activity.

$$pH = -\log[H+]$$

pH provides the needed quantitative information by expressing the degree of the activity of an acid or base in terms of hydrogen ion activity.

The pH value of a substance is directly related to the ratio of the hydrogen ion [H+] and the hydroxyl ion [OH−] concentrations. If the H+ concentration is greater than OH−, the material is acidic; i.e., the pH value is less than 7. If the OH− concentration is greater than H+, the material is basic, with a pH value greater than 7. If equal amounts of H+ and OH− ions are present, the material is neutral, with a pH of 7.

Acids and bases have free hydrogen and hydroxyl ions, respectively. Since the relationship between hydrogen ions and hydroxyl ions in a given solution is constant for a given set of conditions, either one can be determined by knowing the other. Thus, pH is a measurement of both acidity and alkalinity, even though by definition it is a selective measurement of hydrogen ion activity. Since pH is a logarithmic function, a change of one pH unit represents a ten-fold change in hydrogen ion concentration. Table 1 shows the concentration of both the hydrogen ion and the hydroxyl ion at different pH values.

THE MOLAR CONCEPT

A mole of a compound is defined as Avogadro's number of molecules (6.02×10^{23} molecules), which has a mass approximately equal to the molecular weight, expressed in grams. For example, sodium hydroxide, NaOH, which has a molecular weight of 23 + 16 + 1 = 40, would have 40 grams in a mole. Since the atomic weight of the hydrogen ion (H+) is one (1), there is one gram of hydrogen ions in a mole of hydrogen. A solution with a pH of 10 has 1×10^{-10} moles of hydrogen ions, or 10^{-10} grams in a one liter solution.

IONIZATION

An ion is a charged particle, created by an atom or molecule which has either gained or lost electron(s). The presence of ions in solution allows electrical energy to be passed through the solution as a conductor. Different compounds form ions in solution in different amounts, depending on the ability of the atoms to gain or lose electrons. They will dissociate (or ionize) in solution to form hydrogen (H+) or hydroxyl (OH−) ions in the solution.

Molecules that dissociate easily will form strong acids or bases when in aqueous solution (water solvent). Examples of these are hydrochloric acid (HCl) or sodium hydroxide (NaOH):

$$HCl + H_2O \longrightarrow H_3O^+ + Cl^-$$
$$NaOH \longrightarrow Na^+ + OH^-$$

In an aqueous solution, hydrogen ions normally combine with the water solvent to form the hydronium ion (H_3O^+). pH measurements of these solutions are therefore measurements of the hydronium ion concentration. Normally, the terms "hydronium ion" and "hydrogen ion" are used interchangeably in pH measurement applications.

Some compounds form weak acids or bases; only a very small percentage of the compounds dissociates into its constituent ions, so very few hydrogen or hydroxyl ions are formed. An example of this is acetic acid, which forms less than one hydrogen ion for every one hundred molecules:

$$H_2O + CH_3COOH \longrightarrow H_3O^+ + CH_3COO^-$$

Pure water also dissociates weakly, with 10^{-7} hydrogen and 10^{-7} hydroxyl ions formed for every water molecule at 25°C:

$$2H_2O \longrightarrow H_3O^+ + OH^-$$

The addition of acid to water increases the concentration of hydrogen ions and reduces the concentration of hydroxyl ions. A base added to water has the opposite effect, increasing the concentration of hydroxyl ions and reducing the concentration of hydrogen ions:

$$H_2O + HCl \longrightarrow H_3O^+ + Cl^-$$
$$H_2O + NaOH \longrightarrow Na^+ + H_2O + OH^-$$

There is a wide variety of applications for pH measurement. For example, pH measurement and control is the key to the successful purification of drinking water, the manufacture of sugar, sewage treatment, food processing, electroplating, and the effectiveness and safety of medicines, cosmetics, etc. Plants require the soil to be within a certain pH range in order to grow properly, and animals can sicken or die if their blood pH level is not within the correct limits. Figure 1 gives pH values for some common industrial and household products.

pH MEASUREMENT

A rough indication of pH can be obtained using pH papers or indicators, which change color as the pH level varies. These indicators have limitations on their accuracy, and can be difficult to interpret correctly in colored or murky samples.

More accurate pH measurements are obtained with a pH meter. A pH measurement system consists of three parts: a pH measuring electrode, a reference electrode, and a high input impedance meter. The pH electrode can be thought of as a battery, with a voltage that varies with the pH of the measured solution. The pH measuring electrode is a hydrogen ion sensitive glass bulb, with a millivolt output that varies with the changes in the relative hydrogen ion concentration inside and outside of the

pH	H+	OH−
0	(10^0) 1	0.00000000000001 (10^{-14})
1	(10^{-1}) 0.1	0.0000000000001 (10^{-13})
2	(10^{-2}) 0.01	0.000000000001 (10^{-12})
3	(10^{-3}) 0.001	0.00000000001 (10^{-11})
4	(10^{-4}) 0.0001	0.0000000001 (10^{-10})
5	(10^{-5}) 0.00001	0.000000001 (10^{-9})
6	(10^{-6}) 0.000001	0.00000001 (10^{-8})
7	(10^{-7}) 0.0000001	0.0000001 (10^{-7})
8	(10^{-8}) 0.00000001	0.000001 (10^{-6})
9	(10^{-9}) 0.000000001	0.00001 (10^{-5})
10	(10^{-10}) 0.0000000001	0.0001 (10^{-4})
11	(10^{-11}) 0.00000000001	0.001 (10^{-3})
12	(10^{-12}) 0.000000000001	0.01 (10^{-2})
13	(10^{-13}) 0.0000000000001	0.1 (10^{-1})
14	(10^{-14}) 0.00000000000001	1 (10^0)

Table 1

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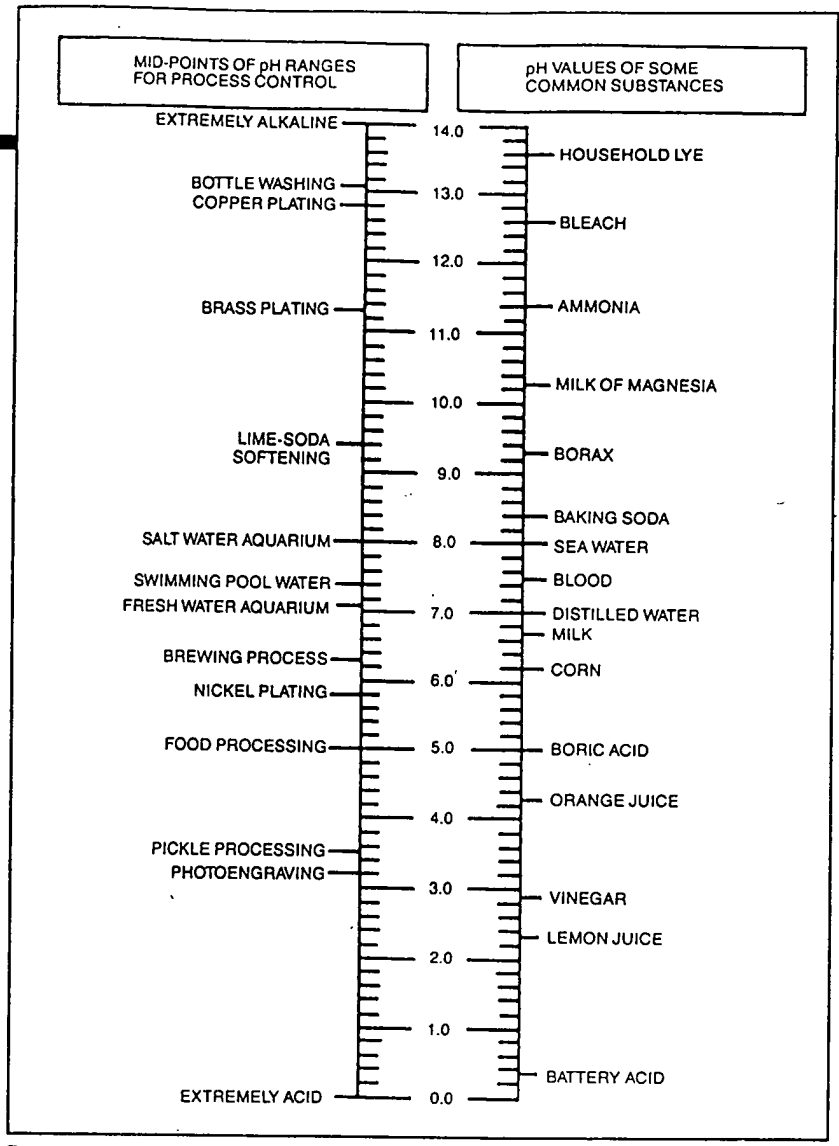


Figure 1

ulb. The reference electrode output oes not vary with the activity of the ydrogen ion. The pH electrode has very igh internal resistance, making the oltage change with pH difficult to ieasure. The input impedance of the H meter and leakage resistances are ierefore important factors. The pH ieter is basically a high impedance mplifier that accurately measures the iinute electrode voltages and displays ie results directly in pH units on either n analog or digital display. In some ases, voltages can also be read for ecial applications or for use with ion-elect or Oxidation-Reduction Potential ORP) electrodes.

EMPERATURE COMPENSATION

mperature compensation is contained ithin the instrument, because pH ectrodes and measurements are mperature sensitive. The temperature ompensation may be either manual or utomatic. With manual compensation, separate temperature measurement is quired, and the pH meter manual ompensation control can be set with the approximate temperature value. With automatic temperature compensation (ATC), the signal from a separate temperature probe is fed into the pH meter, so that it can accurately determine pH value of the sample at that temperature.

BUFFER SOLUTIONS

Buffers are solutions that have constant pH values and the ability to resist changes in that pH level. They are used to calibrate the pH measurement system (electrode and meter). There can be small differences between the output of one electrode and another, as well as changes in the output of electrodes over time. Therefore, the system must be periodically calibrated. Buffers are available with a wide range of pH values, and they come in both premixed liquid form or as convenient dry powder capsules. Most pH meters require calibration at several specific pH values. One calibration is usually performed near the isopotential point (the signal produced by an electrode at pH 7 is 0 mV at 25°C), and a second is typically performed at either pH 4 or pH 10. It is best to select a buffer as close as possible to the actual pH value of the sample to be measured.

TEMPERATURE EFFECTS

As previously stated, the pH electrode is temperature dependent, and may be compensated for in the pH meter circuitry. The circuitry of the pH meter utilizes the Nernst equation, which is a general mathematical description of electrode behavior.

$$E = E_x + \frac{2.3RT_K}{nF} \log (a_i)$$

where:

E_x = constant depending upon reference electrode
R = constant
T_K = absolute temperature (Kelvin)
n = charge of the ion (including sign)
F = constant
a_i = activity of the ion

For pH measurement, we are interested in the hydrogen ion for H+:

$$\frac{2.3RT_K}{nF} = 59.16 \text{ mV}$$

where: n = 1 and T = 25°C. This term is commonly known as the Nernst coefficient. Since pH is defined as the negative logarithm of the hydrogen ion activity, the general equation at any temperature can be expressed as:

$$E = E_x - 1.98\, T_K\, pH$$

Changes in temperature of a solution will vary the millivolt output of the glass pH electrode in accordance with the Nernst equation. Its variation in the electrode sensitivity versus temperature is a linear function, and most pH meters have circuitry designed to compensate for this effect (refer to *Temperature Compensation).* Figure 2 shows the effect on the glass pH electrode signal at various temperatures.

In figure 2, all three slopes intersect at the point of 0 mV and pH 7.0; this implies no millivolt change with temperature at this, the isopotential point. Also, it can be seen that when working near 7.0 pH, temperature compensation is not a significant factor. However, when working at pH levels of 3.0 or 11.0, a temperature change of 15°C can result in an error of 0.2 pH. Since the temperature effect on the electrode has been shown to be linear, the temperature dependence of pH can then be expressed as:

0.03 pH error/pH unit/10°C

The actual pH of the sample can change with temperature due to a change in the hydrogen ion activity in the solution, because ionization of compounds and

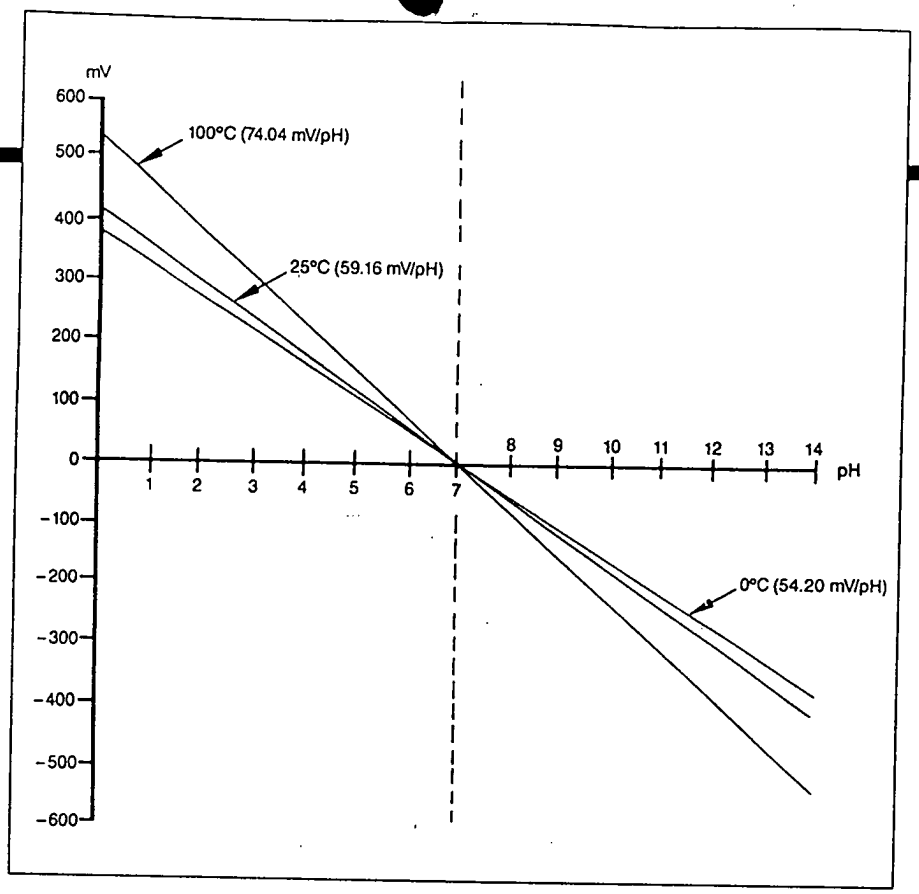


Figure 2

hydrogen ion activity in the solution may be temperature dependent. Temperature compensation does not correct for this, and is not desirable, because an accurate pH measurement is desired at that particular temperature. Temperature compensation only corrects for the change in the output of the electrode, not for the change in the actual solution pH.

Temperature will also affect the glass membrane's impedance. For each 8° below 25°C, the specified impedance approximately doubles. Depending on the original impedance of the glass membrane, the meter will have to handle a higher impedance at a lower temperature.

Written by: OMEGA ENGINEERING, INC.

Measurement of pH

The measurement of pH is one of the most common analytical techniques used in chemistry laboratories today. Nonetheless, pH measurements often suffer from the effects of incorrect materials or incorrect maintenance. The purpose of this paper is to help simplify the choice of materials, methods, and maintenance protocols for pH measurements.

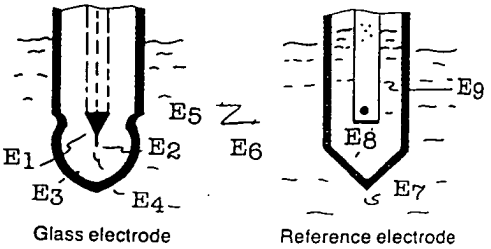
pH MEASUREMENT SYSTEM

A pH measurement system always consists of four parts: a pH sensing electrode, an amplifier that translates the signal into something the user can read, a reference electrode, and the sample being measured. Each part of the system plays a critical role in the measurement process.

A glass electrode is actually a small battery (technically, a transducer). This battery displays a varying voltage, depending upon the pH of the solution in which it is immersed. A reasonable representation of that voltage is given in Figure 1. The potential of the glass electrode is a function of the activity of the free-hydrogen ions and a value E_0 which is supposed to be the 0 or rest potential of the system. This is actually the voltage of the system when the pH is 0.

The reference electrode is also a battery; however, unlike the pH electrode, its voltage does not vary with the activity of hydrogen ion or any other ion solution, but is a function only of the value E_0 or the rest potential.

There are nine actual voltages in the system. Inside the body of the electrode is a wire — normally a silver wire coated with silver chloride. On that wire is some matrix that should present a constant voltage to the wire. At the interface of the wire and solution is a voltage which we can call E_1. Between the wire and the inner surface of the glass is another voltage, on the inner surface of the glass is a voltage (E_3), and across the glass membrane there is a voltage (E_4), which is called the asymmetry potential. There is a voltage on the outer surface of the electrode, a voltage between the pH electrode and the reference electrode; another voltage, referred to as the liquid junction potential or streaming potential, at the point where the filling solution of the reference electrode contacts the sample (E_7); a voltage between the inner surface of the reference electrode and the metal wire that connects the inner filling solution of the reference electrode to the lead wire, and, of course, another voltage on the surface of the connecting wire (E_9).



E_5 — Potential of ion of interest
E_7 — Liquid-junction potential

Figure 1. *Flow chart of selection process for reference electrodes.*

When making a pH measurement, one assumes that all of those voltages remain constant except the voltage on the outer surface of the pH electrode. If that assumption is correct, legitimate pH measurements can be made; if not, then incorrect pH measurements will certainly result. In other words, it is

assumed that the pH electrode delivers a varying voltage to the pH meter, while the reference electrode delivers a constant voltage to the meter.

THE REFERENCE ELECTRODE

The reference electrode is the most complicated part of a pH measurement system. When application problems arise, they normally devolve to the reference electrode. When difficulties in pH measurements are encountered, the source of the problem is typically the reference electrode. In our experience the reference electrode accounts for 70% of the problems that arise in the pH measuring process.

A reference electrode consists of three principal parts: an internal element, which is normally either a silver wire coated with silver chloride or a platinum wire covered with a mixture of calomel (Hg_2Cl_2), some filling solution, and a permeable junction through which the filling solution escapes the electrode (called the fluid junction or liquid junction). The liquid junction can come in several forms, but its principal function is to allow small quantities of the reference electrode's filling solution to slowly leak or migrate into the sample being measured. There are three common forms of this junction: 1) ceramic or other frit material, 2) a fibrous material (the best of which is quartz fiber) or 3) a sleeve junction.

Fritted materials are usually white and are composed of small particles pressed closely together. The filling solution leaks through the open cells between these particles. Since the cells vary considerably in size, the flow rate across the surface is quite variable. In some areas, there is almost no net outward flow of filling solution. At those points the junction is considered to be a "diffusion junction." In the areas where the net outward migration of filling solution is rapid, the electrode is considered to have a flowing junction.

Fiber references come in two types: woven fibers and straight fibers. Woven fibers, such as asbestos fiber, have cells of varying size because of the structure of the woven material. Some of these cells are very small and tightly packed together; at those points there is a diffusion junction. Where the fibers are loosely packed, the flow rate is high and a flowing junction exists.

The quartz fiber reference electrode consists of straight fibers of quartz laid next to each other with straight channels of filling solution passing between them. This junction generally is considered to have no diffusion properties and to be strictly a flowing junction.

The sleeve junction reference electrode is constructed by putting a hole in the side of a glass or plastic tube, grinding the surface around that tube, and covering it with a tapered glass or plastic sleeve. Such a junction is similar in its overall function to a frit junction in that certain areas are pressed tightly and other areas are not, so that both diffusion and flowing junctions exist. A sleeve junction electrode is much faster flowing and much easier to clean than the others.

Reference electrodes are available in a variety of types to accommodate many types of samples. Certain samples require reference electrodes that flow very slowly, whereas other samples require reference electrodes that are easy to clean. The flow chart in Figure 2 should serve as a guide in selecting the reference electrode most appropriate for the application.

The best way to understand the purpose of a reference electrode is to imagine measuring the voltage on a battery with a voltmeter. A voltage measurement cannot be made if only one end of the battery is connected to the meter. If, however, two leads are plugged into the voltmeter and both ends of the battery are touched, a reading is possible.

A pH electrode can be compared to the battery in this example. The wire inside the pH electrode serves the same purpose as the first lead from the voltmeter. The reference electrode can be compared to the second lead, which completes the circuit and enables the measurement of the voltage, or voltage changes, at the pH electrode.

In reality, the pH and reference electrodes are immersed in the same solution with the filling solution of the reference electrode flowing into the sample and completing the circuit with the pH electrode. If the reference electrode is not immersed in the sample, a legitimate measurement is not possible. If the reference electrode immersed in the sample is completely dry, no reading would be forthcoming. If it were filled with filling solution but completely occluded, then it would not establish good consistent electrical connection with the sample, and the readings would vary. A reference electrode that is partially plugged up allows the sample ions to migrate into the junction of the electrode and set up new potentials: voltages that are measured by the system and interpreted as changing pH readings. This is the most common source of problems in a pH measuring system.

The first indication of difficulty in the reference electrode usually is a very long stabilization time. This can be caused by changes in temperature, by reactions taking place in the solution, or by pickup of CO_2 from the atmosphere. Generally, however, a long stabilization time is caused by either the incompatibility of the reference electrode with the sample being measured or by a faulty reference electrode.

It is usually possible to differentiate between drift caused by a faulty electrode and drift caused by other factors (incompatibility between electrode and sample, temperature changes, or reaction within the sample) by moving a hand quickly toward and then away from the electrode. If the reading on the pH meter changes significantly in response to the hand movement, and if the change in the meter reading reverses when retracting the hand, then it would be very safe to assume that the reference electrode is either plugged up or otherwise defective. If the drift continues undisturbed by the movement of the hand toward and away from the electrode, then the problem is probably in the sample. Although this is not a foolproof method, it works most of the time.

There are other ways to check for improperly functioning reference electrodes. The most positive checks are performed using a magnetic stirrer.

- If stirring a sample seems to cause an unstable reading, turn the stirrer off. If the reading changes significantly (by one or two tenths of a pH unit), then there is a reference electrode problem.
- If, while stirring, there is a fair amount of noise (variation in the reading), and turning the stirring motor down to a slower speed reduces the amount of noise, it is safe to assume that there is a reference electrode problem.

If the reference electrode is so dirty that it is completely occluded, it may be just like an open circuit. If this is the case, it exhibits the typical slow, never-ending drift. There are a number of other sources of this same problem (including the electrode's not being plugged in to the meter!), such as: broken wires within the pH or reference electrode; a broken lead wire from the pH or reference electrode; or an open circuit within the meter. A quick way to check whether the problem is in the electrodes or the meter is to substitute new electrodes or, using a wire, paper clip, or shorting plug, short between the reference electrode input and the pH electrode input on the meter. If shorting the electrode inputs does

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pH Control

Accurate measurement and control of pH is a common requirement in industrial plants. Applications include monitoring of cooling tower water, boiler feedwater, process steam, waste treatment, and plant effluent. Control of pH is dependent on measurement reliability, and proper measurement requires an understanding of the basic principles.

By definition, pH is the logarithm of the expression 1/(hydrogen-ion concentration). The concentration is expressed in moles per liter.

The linear scale for pH is not linear with concentration because it is a logarithmic relationship. A change of one pH unit represents a tenfold change in the effective strength of an acid or base.

Control Factors—Normally, one of two conditions exists when controlling pH: either the solution is too acidic and a base must be added to reach a specified higher pH, or the solution is too alkaline and an acid must be added to lower the pH. In both cases, the corrective medium (called a reagent) must be added at a controlled rate.

A key objective in designing pH control systems is to minimize the amount of required reagent. But determining and feeding the exact amount can be difficult because of the logarithmic relationship. Overshooting pH limits by adding more than the correct amount of reagent is easy to do if the control system is improperly designed.

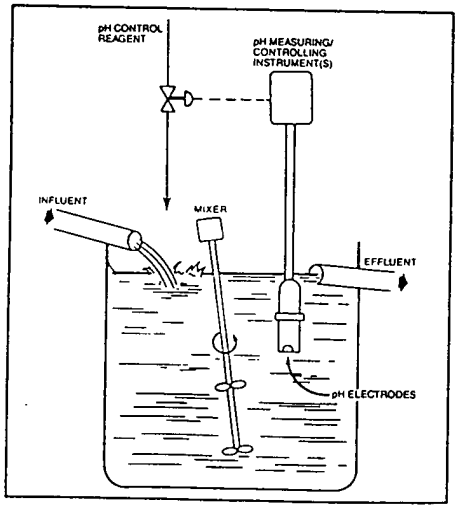

Figure 1. Batch control of pH is normally used when solution volumes are relatively small. Efficient mixing and proper location of pH electrodes is critical to ensure accurate results.

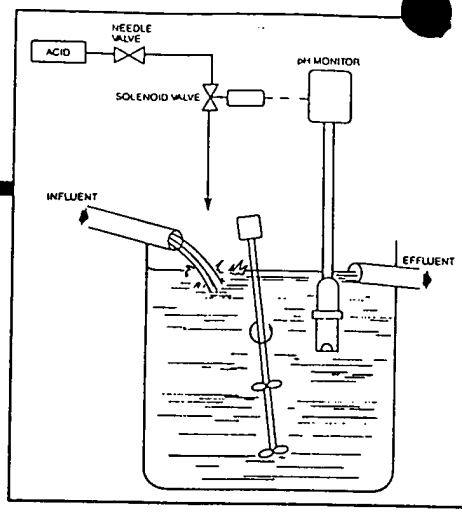

Figure 2. Continuous control of pH involves constant flow of solution in and out of treatment tank.

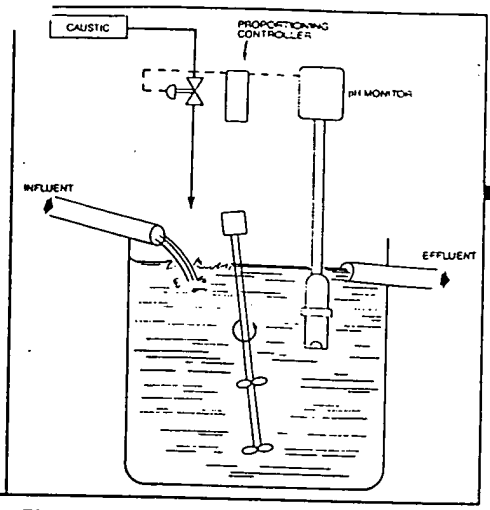

Figure 3. Proportioning controller is used to adjust pH with caustic on this system where influent's pH fluctuates greatly. Throttling valve automatically regulates reagent flow.

Control Techniques—Basically, pH control involves supplying the proper amount of reagent to bring the pH to the desired value. Control can be performed on either a batch or continuous basis.

Batch control is normally used when the total volume of the solution to be treated is relatively low, such as in waste treatment processes where liquids can be collected efficiently and treated in tanks. The amount of reagent required for neutralization can be determined from a titration curve, tank volume, and reaction time. Slow reagent addition rates and good stirring permit more accurate control with less likelihood of pH overshooting.

In the batch process shown in Fig. 1, the tank inlet and reagent feed point are shown located away from the pH electrodes and effluent discharge pipe. This separation is necessary to ensure proper mixing of reagent before measurements are made. Immersed electrodes near the outlet ensure rapid sensor response.

Continuous control is similar to batch control except that there is a continuous flow of influent and treated effluent, Fig. 2. A proportional controller may be required to regulate reagent flow rates if influent pH varies widely, Fig. 3.

Electrode Assembly Placement—An improperly placed electrode assembly can cause excessive deadtime for control action and result in cyclic control and wasted reagent. Deadtime is defined as the elapsed time between reagent addition and the first measureable pH change resulting from the addition. Ideal deadtimes range from 5 to 30 sec. Excessive deadtime can often be avoided by locating the electrode assembly close to where the reagent is added.

Vertical mounting of electrodes is preferred, and they should always be exposed to a representative sample of the process solution. The entire assembly should remain wet at all times to keep the electrodes from drying out.

Because pH is a high-impedance measurement, it is best to utilize a controller, preamplifier or signal conditioner as close to the electrode as possible. The preamplifier converts a high-impedance signal to a low-impedance signal, making it less susceptible to noise and signal loss on transmission back to the receiving instrument over unshielded wire.

Maintenance—A regularly scheduled maintenance program must be enacted to keep electrodes clean and calibrated. Electrode assemblies should be equipped with an ultrasonic cleaning device if solutions contain high levels of suspended solids that are fibrous or crystalline in nature.

Some solutions will chemically attack the electrodes and/or electrode housing material. For example, at elevated temperatures, highly alkaline (pH above 12) solutions can damage glass electrodes or cause significant sodium-ion errors. Fluoride solutions with a pH below 4 will quickly dissolve glass membranes. Process solutions above 230°F will significantly reduce electrode life. Maximum life is normally achieved at ambient temperatures. Coolers are recommended for extremely hot sampling situations.

Based on the article "Understanding pH Measurement and Control" from PLANT ENGINEERING Magazine. Used with permission.

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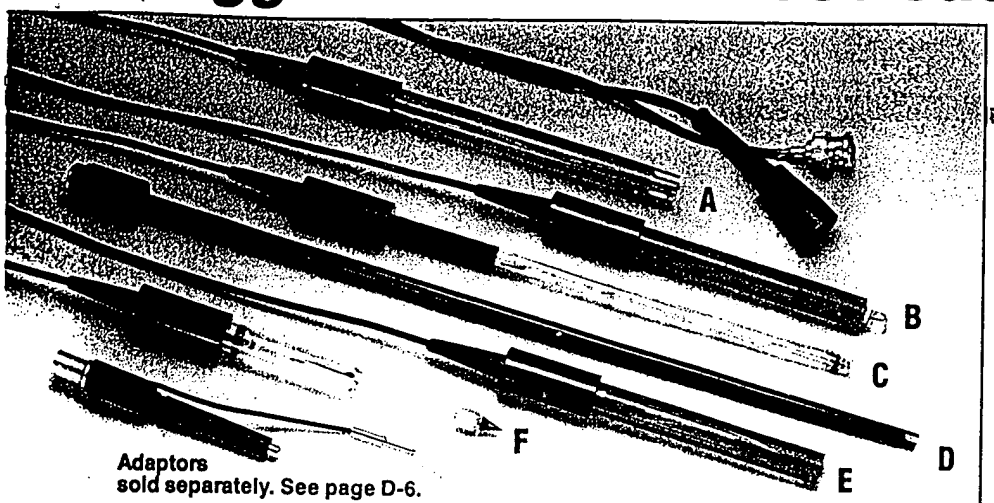
Rugged Gel Filled Electrodes



Adaptors sold separately. See page D-6.

Discount Schedule

1-4 units . . . . . .Net
5-9 units 5%
10-24 units 10%
25 and up 15%

Quantity discounts may be applied to assorted quantities. Discount schedule applies to page D-6 thru D-12 and D-20.

	Part No. BNC	Part No. U.S. Std.	Application	Insertion Length (mm)	Diameter (mm)	pH Range	Temp. °C
A	PHE-1311	PHE-1311-U	General Purpose	110	12	0-12	– 5 to 80
A	PHE-1411	PHE-1411-U	General Purpose for Samples Requiring Double Junction	110	12	0-12	– 5 to 80
A	PHE-1511	PHE-1511-U	For use with sulfides or other contaminants found in plating baths and process streams	110	12	0-12	– 5 to 80
B	PHE-1312	PHE-1312-U	General Purpose with removeable bulb guard	110	12	0-12	– 5 to 80
B	PHE-1412	PHE-1412-U	Double junction design for use with interfering ions such as zinc, copper or sulfide.	110	12	0-12	– 5 to 80
C	PHE-1332	PHE-1332-U	Test Tubes	180	6.5	0-12	– 5 to 80
C	PHE-1432	PHE-1432-U	Test Tubes for samples requiring double junction	180	6.5	0-12	– 5 to 80
D	PHE-1335	PHE-1335-U	Extra long Test Tubes (detachable style shown)	300	6	0-13	0-100
E	PHE-1371	PHE-1371-U	Measurement of flat, moist surfaces such as meat or paper	110	12	0-12	– 5 to 80
E	PHE-1471	PHE-1471-U	Measurement of flat surfaces for samples requiring double junction	110	12	0-12	– 5 to 80
F	PHE-2381	PHE-2381-U	Extra rugged puncture tip for meats, cheeses, fruits, leather	55	8	0-10	– 5 to 100
F	PHE-2881	PHE-2881-U	Extra rugged puncture tip (Calomel)	55	8	0-10	– 5 to 60
F	PHE-2481	PHE-2481-U	Extra rugged puncture tip for samples requiring double junction	55	8	0-10	– 5 to 100
G	PHE-2385	PHE-2385-U	Rugged puncture tip for meats, cheeses, fruits, leather	55	8	0-13	0-100
H	PHE-1317	PHE-1317-U	Economical with removeable guard and Teflon® junction	110	12	0-13	0-100
H	PHE-1417	PHE-1417-U	Economical with double Teflon® junction	110	12	0-12	0-80
J	PHE-1304	PHE-1304-U	Economy	90	12.5	0-12	0-80
K	PHE-1301	PHE-1301-U	Economy	89	13	0-12	0-80
L	ORE-1311	ORE-1311-U	General Purpose-ORP	110	12	± 5000 mV	– 5 to 80
L	ORE-1411	ORE-1411-U	Dbl. junction for interfering ions such as zinc, copper or sulfide-ORP	110	12	± 5000 mV	– 5 to 80
L	ORE-1511	ORE-1511-U	For use with sulfides or other contaminants found in process streams-ORP	110	12	± 5000 mV	– 5 to 80

All electrodes supplied with 3 ft cable. For other configurations, see page D-4.
For additional lead length add desired length as suffix to electrode number and add $1 per additional foot.

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Thermocouple Reference Junction Principles

THEORY: When accurate thermocouple measurements are required, it is common practice to reference both legs to copper lead wire at the ice point so that copper leads may be connected to the emf readout instrument. This procedure avoids the generation of thermal emfs at the terminals of the readout instrument. Changes in reference junction temperature influence the output signal and practical instruments must be provided with a means to cancel this potential source of error. The EMF generated is dependent on a difference in temperature, so in order to make a measurement the reference must be known. This is shown schematically in Fig. #1 and can be accomplished by placing the reference junction in an ice water bath at a constant 0°C (32°F). Because ice baths are often inconvenient to maintain and not always practical, several alternate methods are often employed.

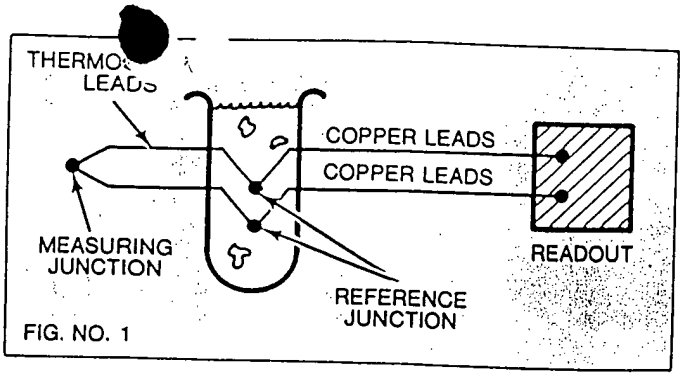

FIG. NO. 1

ELECTRICAL BRIDGE METHOD: This method usually employs a self-compensating electrical bridge network as shown in Figure 2. This system incorporates a temperature sensitive resistance element (R_T), which is in one leg of the bridge network and thermally integrated with the cold junction (T_2). The bridge is usually energized from a mercury battery or stable d.c. power source. The output voltage is proportional to the unbalance created between the pre-set equivalent reference temperature at (T_2) and the hot junction (T_1). In this system, the reference temperature of 0°C or 32°F may be chosen.

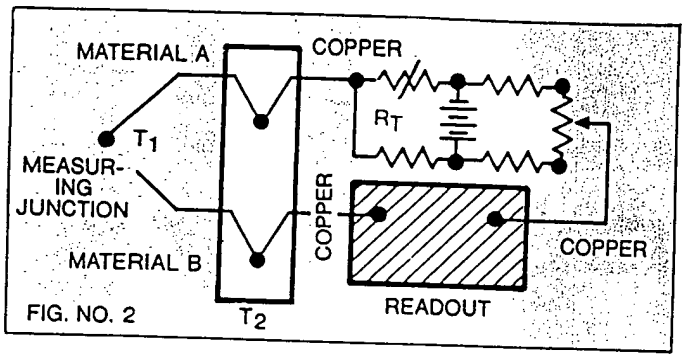

FIG. NO. 2

As the ambient temperature surrounding the cold junction (T_2) varies, a thermally generated voltage appears and produces an error in the output. However, an automatic equal and opposite voltage is introduced in series with the thermal error. This cancels the error and maintains the equivalent reference junction temperature over a wide ambient temperature range with a high degree of accuracy. By integrating copper leads with the cold junction, the thermocouple material itself is not connected to the output terminal of the measurement device, thereby eliminating secondary errors.

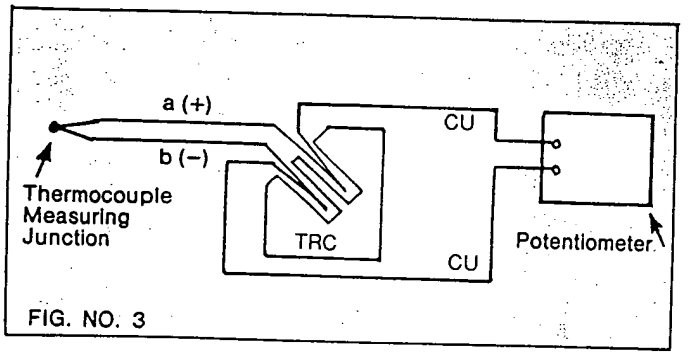

FIG. NO. 3

THERMOELECTRIC REFRIGERATION METHOD: The Omega TRC Thermoelectric Ice Point Reference Chamber relies on the actual equilibrium of ice and distilled, deionized water and atmospheric pressure to maintain several reference wells at precisely 0°C. The wells are extended into a sealed cylindrical chamber containing pure distilled, deionized water. The chamber outer walls are cooled by thermoelectric cooling elements to cause freezing of the water in the cell. The increase in volume produced by freezing an ice shell on the cell wall is sensed by the expansion of a bellows which operates a microswitch, de-energizing the cooling element. The alternate freezing and thawing of the ice shell accurately maintains a 0°C environment around the reference wells. An application schematic is shown in Fig. #3.

Completely automatic operation eliminates the need for frequent attention required of common ice baths. Thermocouple readings may be made directly from ice point reference tables, such as those listed in the technical section, without making corrections for reference junction temperature. Any combination of thermocouples may be used with this instrument by simply inserting the reference junctions in the reference wells. Calibration of other type temperature sensors at 0°C may be performed as well.

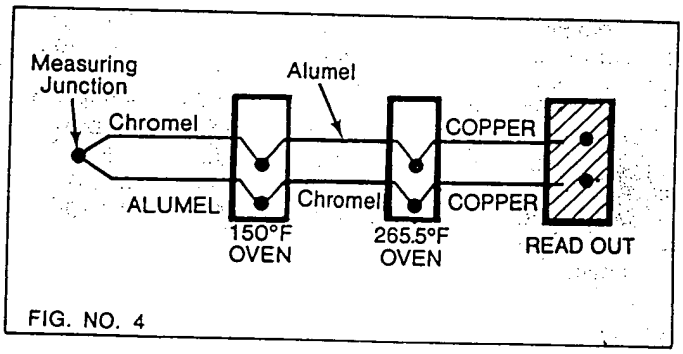

FIG. NO. 4

HEATED OVEN REFERENCES:
The double-oven type employs two temperature-controlled ovens to simulate ice-point reference temperatures as shown in Fig. 4. Two ovens are used at different temperatures to give the equivalent of a low reference temperature differing from the temperature of either oven. For example, leads from a Chromel-Alumel thermocouple probe are connected with a 150° oven to produce a Chromel-Alumel and an Alumel-Chromel junction at 150°F (2.66 mv each).

The voltage between the output wires of the first oven will be twice 2.66 mv or 5.32 mv. To compensate for this voltage level, the output leads (Chromel and Alumel) are connected to copper leads within a second oven maintained at 265.5°F. This is the precise temperature at which Chromel-Copper and Alumel-Copper produce a bucking voltage differential of 5.32 mv. Thus, this voltage cancels out the 5.32 mv differential from the first oven leaving 0 mv at the Copper output terminals. This is the voltage equivalent of 32°F (0°C).